GR-CPCI-GR740 Letter of Volatility

Letter of Volatility 2023-09-28

Doc. No GR-CPCI-GR740-LOV

Issue 1.1

CHANGE RECORD

Issue	Date	Section	Description
1.0	2023-05-26	All	First issue of this document.
1.1	2023-09-28	1.2, 1.4, 3.1, 3.6	1.2: Removed “www” from web links. 1.4: Expanded the definition of “power cycle”. 3.1: “I2C device” changed to “I2C controller” 3.6: FT4232H also provides access to on-board power monitors. Corrected format for serial number programmed into EEPROM.

1 INTRODUCTION

1.1 Scope of the document

This document is a Letter of Volatility for the GR-CPCI-GR740 development board [RD1]. It applies to revision 1.5 and earlier of the product.

1.2 Reference documents

[RD1] GR-CPCI-GR740-UM, “GR-CPCI-GR740 Development Board User Manual”, https:/gaisler.com/gr-cpci-gr740

[RD2] GRMON3-UM,”GRMON3 User’s Manual”, https://gaisler.com/doc/grmon3.pdf

[RD3] GR740-UM-DS, “GR740 Datasheet and User’s Manual”, https://gaisler.com/gr740

1.3 Abbreviations

b	Bit
B	Byte (8 bits)
DRAM	Dynamic Random Access Memory
EEPROM	Electrically Erasable Programmable Read-Only Memory
FPGA	Field-Programmable Gate Array
Ki	Kibi (2^{10}=1024)
Mi	Mebi (2^{20}=1048576)
OTP	One-Time Programmable
PID	Product ID
RAM	Random Access Memory
SDRAM	Synchronous Dynamic Random Access Memory
SODIMM	Small Outline Dual In-Line Memory Module
SPD	Serial Presence Detect
SRAM	Static Random Access Memory
USB	Universal Serial Bus
VID	Vendor ID

1.4 Terms and Definitions

Power cycle: The process of removing the external 5 V power input from the board, keeping it removed for a minimum of 10 s, and later restoring the power input.

Volatile memory: Memory that requires power to retain its contents.

Non-volatile memory: A memory that retains its contents without a source of power.

User Accessible memory: A memory that can be written by use of the GRMON debug software [RD2] or user application software running inside the GR740 [RD3].

2 SUMMARY

2.1 Volatile memory

Device/Function	Type	Size	User Accessible	Sanitization Procedure
GR740 internal memory (L2-cache, L1-caches, FIFOs, registers)	SRAM and flip-flops	<3 MiB	Yes	Power cycle
External RAM for GR740	SODIMM SDRAM	512 MiB	Yes	Power cycle
IGLOO FPGA dynamic data	SRAM and flip-flops	36 Kib	No	Power cycle
FT4232H USB-Serial converter	Internal RAM		No	Power cycle

All volatile memory on the GR-CPCI-GR740 can be erased by removing 5 V power from the board for a time of 10 s or longer. The board does not contain any battery or other power sources.

2.2 Non-volatile memory

Function	Type	Size	User Accessible	Sanitization procedure
Boot memory for GR740	Flash	8 MiB	Yes	Section 2.3
IGLOO FPGA configuration memory.	FPGA	125 k gates	No	None
Versa-clock startup configuration	OTP EPROM	<500 B	No	None
SODIMM SPD parameters	EEPROM	128 B/SODIMM	No	None
FT4232H configuration parameters[1]	EEPROM	128 B	No[2]	None

1. Only present on revision 1.5 and later of the GR-CPCI-GR740.
2. Not User Accessible per section 1.4, but reprogrammable with commonly available software and hardware. For default contents at delivery see section 3.6.

2.3 Sanitization procedure for GR740 boot memory

Requirements: GRMON2 or GRMON3 debug software [RD2]

1. Place all JP11 jumpers in position A-B (there are 22 such jumpers in total).
2. Verify that no jumper is installed in position 1-2 of JP6.
3. Verify that jumpers are installed in positions 3-4, 5-6, 7-8, 9-10, and 11-12 of JP6.
4. Apply pull-down to GPIO[15] and GPIO[10] using the front-panel DIP switch (see section 4.4 “Front Panel” in [RD1]).
5. Apply power to the board.
6. Connect the GRMON debug monitor software to the GR-CPCI-GR740 using any supported debug link. For details refer to section 4.15 in [RD1].
7. In the GRMON command prompt run the command “`info reg gpreg1::ftmfunc`” and verify that this register has the value `0x003fffff`.
8. In the GRMON command prompt run the command “`flash unlock all`” followed by the command “`flash erase all`”.

The expected output from GRMON3 is shown below:

```
grmon3> info reg gpreg1::ftmfunc
  General Purpose Register Bank
      0xffa0b000  FTMCTRL function enable register        0x003fffff

grmon3> mcfg1
  mcfg1: 0x000000ff

grmon3> flash unlock all
  Unlock in progress
  Block @ 0xc07e0000 : code = 0x80  OK
  Unlock complete

grmon3> flash erase all
  Erase in progress
  Block erase @ 0xc07e0000 : code = 0x80  OK
  Erase complete

grmon3> mem 0xc0000000
  0xc0000000  ffffffff  ffffffff  ffffffff  ffffffff    ................
  0xc0000010  ffffffff  ffffffff  ffffffff  ffffffff    ................
  0xc0000020  ffffffff  ffffffff  ffffffff  ffffffff    ................
  0xc0000030  ffffffff  ffffffff  ffffffff  ffffffff    ................
```

3 DETAILED DESCRIPTION

3.1 SDRAM SODIMMs

The GR-CPCI-GR740 comes with two detachable SODIMM modules providing external RAM for the GR740. Each is equipped with 256 MiB of volatile SDRAM and 128 B of non-volatile SPD EEPROM. The SDRAM is User Accessible and can be sanitized by removing power from the board.

The SPD EEPROMs are not user accessible per the definition in section 1.4. However, the EEPROMs could in theory be written by unplugging the SODIMMs from the GR-CPCI-GR740 and connecting them to a custom I2C controller.

3.2 GR740

A single GR740 ASIC [RD3] is mounted on the board. It contains volatile memory in the form of (approximately) 2.9 MiB of SRAM (most of which forms the L2-cache) and 182 Kib of flip-flops. This memory can be erased by power cycling the device. The GR740 does not contain any non-volatile memory.

3.3 Boot PROM for GR740 (28F640J3)

An 8 MiB non-volatile flash memory (28F640J3) is mounted on the board and connected to the GR740. This component provides a boot PROM for the GR740, see section 4.5 “Memory” in [RD1] for more information.

This non-volatile memory is User Accessible and a sanitization procedure is provided in section 2.3.

3.4 IGLOO FPGA (AGLN125)

A single AGLN125 IGLOO FPGA is mounted on the GR-CPCI-GR740. At board delivery, this device is programmed to perform a PCI arbiter function and to manage parameters for the VersaClock (section 3.5) via an I2C interface, refer to section 4.8 “FPGA for PCI Arbiter & Versaclock Controller” in [RD1] for more information.

The AGLN125 is a flash-based FPGA and therefore the configuration memory (corresponding to 125k logic gates) is non-volatile. The device is not User Accessible per the definition in section 1.4. However, the memory could in theory be read and written by connecting an FPGA programming tool to the J13 header on the GR-CPCI-GR740. Doing so would in most cases render the PCI, SDRAM, and Ethernet interfaces of the GR-CPCI-GR740 non-functional.

3.5 VersaClock programmable clock generator (5P49V5901)

Two copies of the 5P49V5901 are mounted on the GR-CPCI-GR740. They generate clock signals with precise relative delays for the board’s SDRAM and Ethernet interfaces. The device is programmable through an I2C interface that provides access to OTP configuration bits (total information content <500 B). The I2C interfaces are connected directly to the IGLOO FPGA (section 3.4) and are not User Accessible per the definition in section 1.4.

3.6 FT4232H USB-Serial converter and configuration EEPROM

A single FT4232H is mounted on the GR-CPCI-GR740 and provides access to the GR740 JTAG and UART interfaces, as well as on-board I2C power monitors, via the front-panel USB port. On boards with revision 1.5 and higher, a 128 B EEPROM is connected to the FT4232H device. On boards with revision 1.4 and lower, no EEPROM is present.

Neither the FT4232H, nor the EEPROM connected to it, are User Accessible per the definition in section 1.4. But, if present, the EEPROM can be reprogrammed from any computer connected to the USB port of the GR-CPCI-GR740; if that computer has the appropriate software installed.

At board delivery the EEPROM is programmed with the following settings:

USB VID/PID: `0403:6011` (FTDI Default)

Manufacturer: “`Frontgrade Gaisler AB`”

Product Description: “`GR-CPCI-GR740`”

Serial Number: “GR740C*nnnn*”, where “*nnnn*” is the 4-digit serial number of the board.