GR718B in Cold-Spare Scenarios

Application note 2016-11-29

Doc. No GR718B-AN-0001

Issue 1.1

CHANGE RECORD

Issue	Date	Section / Page	Description
1.0	2016-11-24		First issue of this application note.
1.1	2016-11-28	Section 3,4 and 6	Minor clarifications and added schematics for resistors and capacitors

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1 INTRODUCTION

1.1 Scope of the Document

This document establishes the application note for scenarios in which the GR718B is used in cold-spare-like conditions.

The work has been performed by Cobham Gaisler AB, Göteborg, Sweden.

1.2 Reference Documents

The following documents are referred as they contain relevant information:

[RD1] GR718B Data Sheet and User's Manual

2 ABBREVIATIONS

LVDS	Low-voltage differential signaling
IO	External Input or Output pin
VDDIO	External Supply Voltage for external Inputs and output pins
ESD	Electrostatic discharge
PCB	Printed circuit board
WCA	Worst-Case Analysis
PSA	Parts Stress Analysis
FMECA	Failure mode, effects and criticality analysis
OVP	Over-voltage protection

3 INTRODUCTION

When connecting a GR718B LVDS port to a circuit that is not power supplied by the (galvanically) same 3.3V supply as VDDIO on the GR718B, it is important to consider the I/O-port ratings of the GR718B. A fully powered GR718B does not put any restrictions on the other circuit's LVDS port (assuming non-failure case). However, when GR718B is not powered, while the other circuit is powered, it is important to note that the GR718B LVDS ports have no integrated cold-spare functionality. All I/O pins on the GR718B, including the LVDS I/O pins, have ESD-protection diodes to ground and to VDDIO. The ESD diode to VDDIO will start to conduct current whenever any I/O pin goes above VDDIO. If the I/O voltage does not exceed the maximum VDDIO+0.3V, and the ESD diode current is less than 10mA, then the Absolute Maximum Rating table is not violated. It should however be noted that this only guarantees that GR718B is not damaged. The GR718B is not guaranteed to provide any functionality, and an invalid LVDS signal is likely to be observed at the inputs, since this is outside the recommended operating conditions. When the GR718B is used in applications with system supply conditions as described above, its LVDS inputs can go outside the absolute maximum limits. This can be avoided by adding protective networks on the GR718B LVDS pins as described in this application note.

For more information about the GR718B device see GR718B Data Sheet and User's Manual.

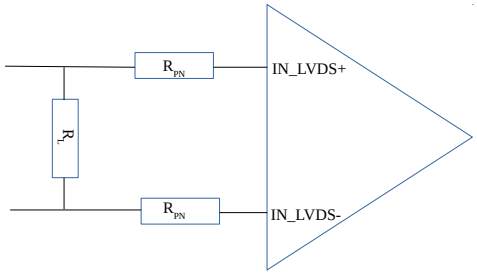
4 PROTECTIVE NETWORK ON GR718B LVDS INPUTS

A resistor in series with each LVDS input pin can be added, which should limit the maximum current to 10mA during all possible combinations of supply voltage conditions that can occur in the system. A straightforward method to determine the worst-case minimum value of this resistor is to establish the maximum supply voltage that exists to any of the interconnected circuits. In this example we assume maximum 3.6V for all supply voltages to all interconnected circuits, and no negative supply voltage exists in this part of the system. This means that the maximum worst-case voltage across the protection resistors cannot exceed 3.6V. Thus, the resistance value can safely be chosen to R_{PN} = 3.6V/10mA = 360Ω (min).

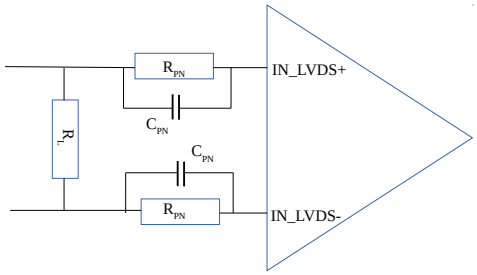
However, inserting a series resistor will also introduce an additional settling delay in the signal path, which will reduce the eye-diagram opening when high speed is of importance. In cases where the eye-opening becomes too small, it is either advisable to further optimize the above resistance calculations, or a capacitor can be put in parallel with each protection resistor, which will pass the signal on to the LVDS input without added settling delay. Optimizing the resistance value will lead to a trade-off between signal integrity and protection effectiveness, whereas adding a capacitor is always beneficial, at the cost of increased PCB area. The value of the capacitance should be an order of magnitude larger than the LVDS input capacitance plus the PCB parasitic capacitance.

Therefore, the protective network should be placed as close to the LVDS receiver input pins as possible, in between the 100Ω termination resistor and the LVDS input pins. The maximum capacitance of a GR718B LVDS input pin is 5pF, and the PCB layout should be designed to not add

more than another 5pF, which results in a total of less than 10pF. This means that a 100pF capacitor added in parallel with each protection resistor may give a good result. But a more accurate timing analysis should be made if the timing of a certain LVDS link is critical.



Drawing 1: Protective network for LVDS inputs using series resistor



Drawing 2: Protective network for LVDS inputs using series resistor and capacitor

5 PROTECTIVE NETWORK ON GR718B LVDS OUTPUTS

The GR718B LVDS Output does not need any protective network if the LVDS receiver in the other end has a cold-spare input. If it is not a cold-spare input in the other end, that input may very well need to be protected from getting too high ESD-diode currents, which in this case would come from the GR718B LVDS output driver.

6 FAILURE PROPAGATION

If an LVDS link should be protected from failure propagation (e.g. if it is part of a cross-coupling interface), and at least one of the LVDS links ends is non-cold-spare, a protective network must be inserted in series in the LVDS link. The resistance value is calculated for maximum current in the same way as above, but here, the worst-case maximum fault supply voltage should be applied in the calculations.

If the application case requires the LVDS interface to be failure-propagation protected at the same time as high speed is required, it is recommended to add capacitors in parallel to the protection resistors. Then and only then, the value of the resistors can be chosen high enough to limit the maximum fault current driven by supply voltages significantly higher than 3.6V.

Supply transients, occurring before the over-voltage protection (OVP) in a faulty power supply shuts down the supply, should also be taken into account in the calculations of the protective network. An example of a protective network, assuming a supply of $3.3V_{nom}$ and fault transient voltage limited to $4V_{peak}$, results in a resistor value of minimum R_{PN} = 400Ω (464Ω standard value), and a parallel capacitor of 100pF if high speed is of importance. But detailed system analyses – WCA, PSA and FMECA – should determine the final choice of values. And in the same way as above, these resistors and capacitors should always be placed very close to the LVDS input pins.