GR-CPCIS-XCKU Data Sheet and User's Manual

GR-CPCIS-XCKU

Baseline features

The GR-CPCIS-XCKU is an FPGA development board. Its cutting-edge technology allows the development of next-generation system on chips and its interfaces are particularly suited to emulate space applications.

This board implements a Xilinx Ultrascale FPGA, in a 1517 ball-grid-array package. The board was initially designed to use a XCKU060 sized device but is compatible with larger devices of the same series with the same footprint.

Optionally, the board also features a GR716 rad-hard microcontroller which can act as the FPGA supervisor for scrubbing and programming.

The GR-CPCIS-XCKU is a 1 slot, 6U high board with a CPCI-S backplane format, and can be used stand alone on the bench top, or installed in a CPCI-Serial rack

The GR-CPCIS-XCKU includes:

- Xilinx XCKU, in 1517 pin FCBGA package.
- GR716 microcontroller. - Optional
- FPGA interface to DDR3 SDRAM via two SODIMM connectors.
- SPI flash for FPGA configuration (512 Mbit), for GR716 boot (256 Mbit), and for data (256 Mbit). The FPGA has also access to two NVM: 512 Mbit SPI and Parallel Flash memory (40 bit wide)
- FMC Mezzanine expansion connector.
- Scrubbing interface for FPGA. Available also without the GR716.
- 2×10 connector to interface with a GR-ACC-6U_6UART breakout board providing access to 6 UARTS (or 16 GPIOs).

Front Panel interfaces

- 2x RJ45 to FPGA via magnetics and Gbit Ethernet transceivers. RGMII interface to FPGA
- 1x eSATA for SpaceFibre to FPGA via CML redriver.
- 2x MDM9 for SpaceWire via LVDS transceivers/repeaters to FPGA.
- Status LEDs, push-buttons and switches
- 2xSMA or 2xSMB for PPS time distribution to FPGA.
- 2xUSB ports for:
    - JTAG access to FPGA and FMC (separate chains)
    - GR716 debug UART and two FPGA UARTs

Backplane interfaces

- 8 x SpaceFibre for full-mesh interconnect using FPGA GTH banks
- 8 x SpaceWire for dual-star interconnect
- Dual-redundant CAN-bus to FPGA and/or GR716 via two or four transceivers
- SGPIO and I2C connected to FPGA with jumper-configurable pull-ups
- 12V supply from backplane that can be turned off by the external input PS_ON#
- Other utility signals connected to the FPGA

This board design is part of a project that has received funding from the *European Union's Horizon 2020 research and innovation programme* under Grant Agreement No 869945.

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1 INTRODUCTION

1.1 Scope of the Document

This document provides a Data Sheet & User Manual for the *GR-CPCIS-XCKU* Development and Demonstration board.

The work has been performed by Frontgrade Gaisler AB, Göteborg, Sweden.

1.2 Reference Documents

The following documents are referred as they contain relevant information:

[RD1] GR-CPCIS-XCKU Board_schematic.pdf, Schematic

[RD2] GR-CPCIS-XCKU Board_assy_drawing.pdf, Assembly Drawing

[RD3] GRMON3 User's Manual, available from: https://www.gaisler.com/index.php/products/debug-tools/grmon3

[RD4] GR716 LEON3FT Microcontroller - User's Manual, available at https://www.gaisler.com/doc/gr716/gr716-ds-um.pdf

2 ABBREVIATIONS

ASIC	Application Specific Integrated Circuit.
DSU	Debug Support Unit
EDAC	Error Detection and Correction
ESA	European Space Agency
ESD	Electro-Static Discharge
FMC	FPGA Mezzanine Card
FPGA	Field Programmable Gate Array
GPIO	General Purpose Input / Output
HSSL	High Speed Serial Link
IC	Integrated Circuit
I/O	Input/Output
IP	Intellectual Property
LDO	Low Drop-Out
LPC	Low Pin Count
LVDS	Low Voltage Digital Signalling
PCB	Printed Circuit Board
POL	Point of Load
PPS	Pulse Per Second
SOC	System On a Chip

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SPW	SpaceWire
TBC	To Be Confirmed
TBD	To Be Defined

3 INTRODUCTION

3.1 Overview

This document describes the *GR-CPCIS-XCKU* Development Board.

PLEASE READ SECTION 3.2 BEFORE USING THE BOARD.

This equipment is a 1 slot, 6U high board with a CPCI-S backplane format. It can be used stand alone or it can be installed in a CPCI-Serial rack.

The Ultrascale FPGA allows the development of next-generation system on chips on FPGA while also providing a fantastic benchmark for FPGA prototypes for ASIC products.

This board also provides developers with a convenient hardware platform for the evaluation and development of software for the GR716 radiation hardened microcontroller.

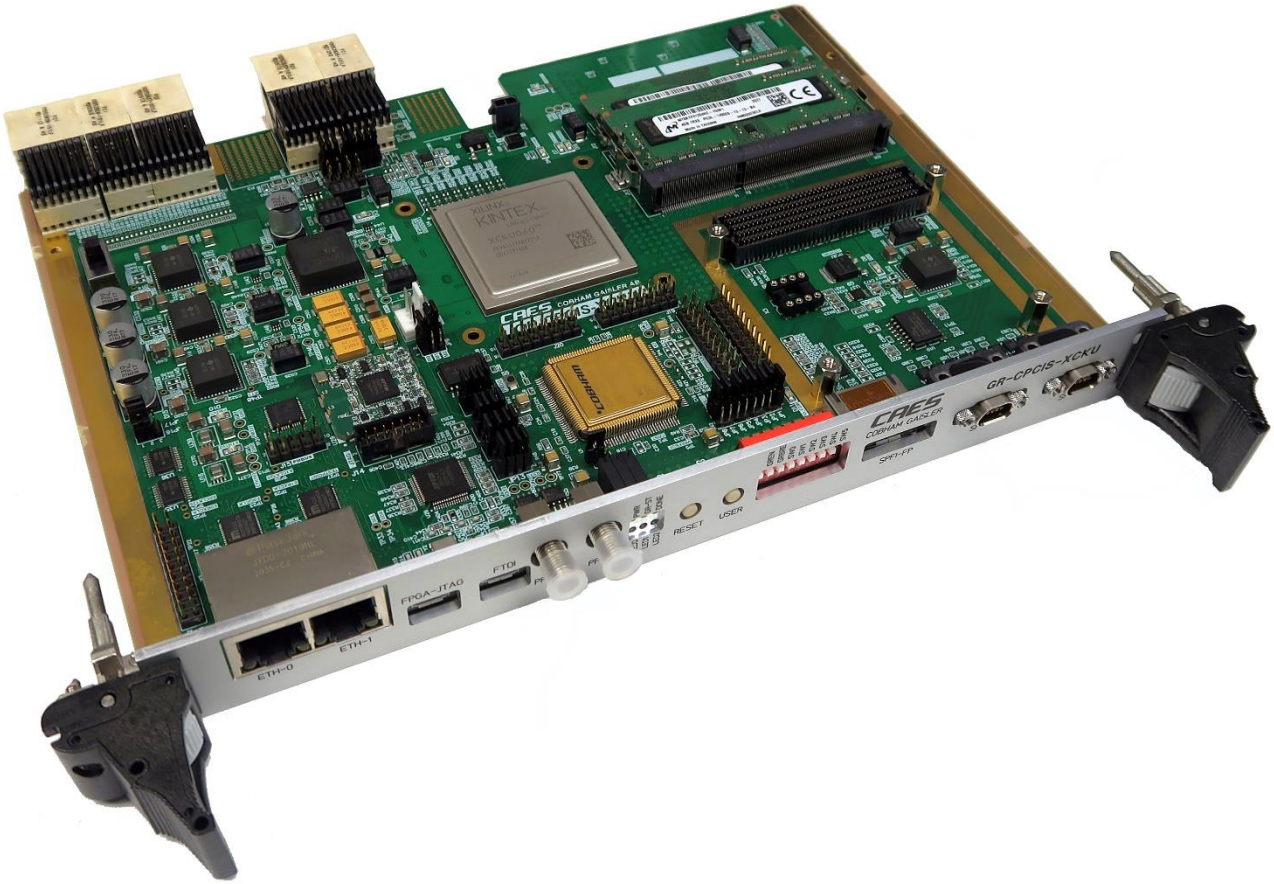

Figure 1 GR-CPCIS-XCKU Development Board

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The board contains the following main items as detailed in section 4 of this document:

- Frontgrade Gaisler GR716 radiation-hardened microcontroller featuring a fault-tolerant LEON3 SPARC V8 processor (Note: This item is not fitted in some versions of the board)
- Xilinx Ultrascale XCKU060 FPGA
- Dual SODIMM sockets for DDR3 SDRAM memory (96 bit wide interface)
- 512 Mbit SPI memory (Cypress, S25FL512SAGN in SOIC-16 package) for FPGA configuration
- 512 Mbit SPI memory (Cypress, S25FL512SAGN in SOIC-16 package) for FPGA non-volatile memory
- 512 Mbit SPI memory (Cypress, S25FL512SAGN in SOIC-16 package) for GR716-boot configuration
- 512 Mbit SPI memory (Cypress, S25FL512SAGN in SOIC-16 package) for GR716-data non-volatile memory
- Parallel Flash memory (40 bit wide) connected to FPGA
- Dual Gbit Ethernet interface with standard RJ45 connector
- Dual 1 PPS interface
- Dual SPW/LVDS interfaces with MDM9S connector on front panel
- front panel SPFI interface with E-SATA connector
- FTDI Serial to USB converter for FMC- JTAG and GR716 DSU/UART interfaces
- FMC mezzanine connector
- Header for FPGA SOCPIO (16 pins)
- Header for GR716 SOCPIO (30 pins)
- CPCI-S Backplane interface
- VIN power input (+12V nom.) via backplane or 2 pin header
- on-board regulators converting from VIN to various on-board voltages
- switches and headers for bootstrap and configuration settings

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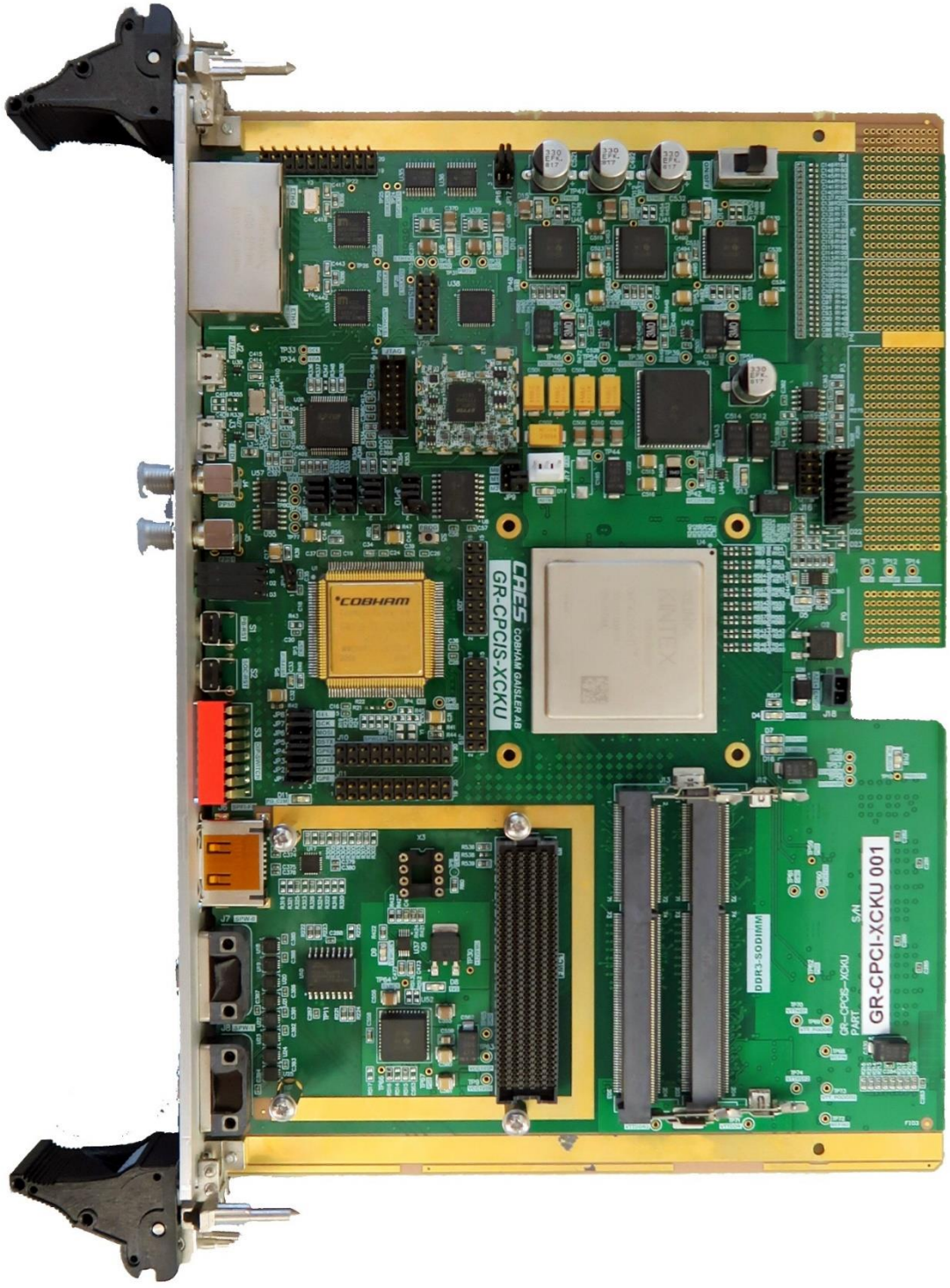

Figure 2 GR-CPCIS-XCKU Main Board

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3.2 Handling

ATTENTION: OBSERVE PRECAUTIONS FOR HANDLING ELECTROSTATIC SENSITIVE DEVICES

This unit contains sensitive electronic components which can be damaged by Electrostatic Discharges (ESD). When handling or installing the unit observe appropriate precautions and ESD safe practices.

When not in use, store the unit in an electrostatic protective container or bag.

When configuring the jumpers on the board, or connecting/disconnecting cables, ensure that the unit is in an unpowered state.

WARNING: Before powering up the board, please mount the FPGA cooling fan included in the delivery kit.

[For S/N 001,002,003] When operating the board in a 'stand-alone' configuration, the power supply should be current limited to prevent damage to the board or power supply in the event of an over-current situation.

[For other S/N] When operating the board in a 'stand-alone' configuration , only use the power supply included in the delivery kit.

This board is intended for commercial use and evaluation in a standard laboratory environment, nominally, 20°C. All devices are standard commercial types, intended for use over the standard commercial operating temperature range (0 to 70°C).

4 BOARD DESIGN

4.1 Board Block Diagram

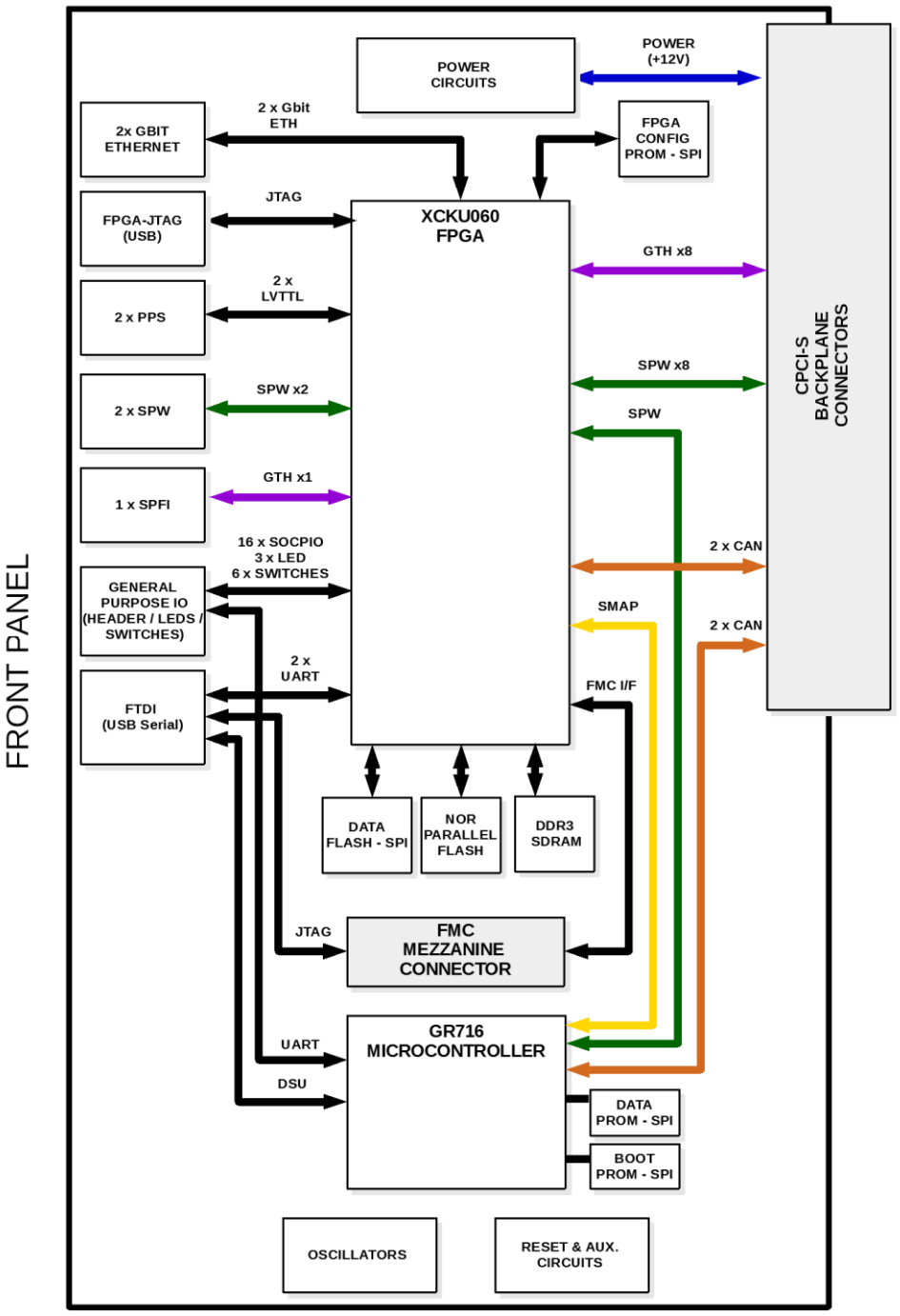

Figure 3 GR-CPCIS-XCKU Board Block Diagram

The *GR-CPCIS-XCKU* Board provides the electrical functions and interfaces as represented in the block diagram, Figure 3.

4.2 Board Mechanical Format

The design is conceived as a 6U high, 1 slot wide module for mounting in the controller slot of a 6U rack with a CPCI-S Backplane.

The dimensions of the main PCB are 233.35x160mm (excluding the connector protrusions).

The board can be fitted with a front-panel compatible with either a 20.32mm or 25.4mm wide backplane pitch. The default panel is for a 25.4mm backplane pitch.

This prototype board is intended for installation in a rack with forced air cooling. However, for installation in conduction cooled environment, a future design could accommodate standard wedgeloks on the top and bottom rail edges of the board.

This would require the exact Wedge-lok type and mounting hole definition to be known, and the front panel to be modified to accommodate them.

A standard FMC style (VITA 57.1) mezzanine interface connector allows an FMC -LPC Mezzanine board to be mounted to the board.

The face to face mounting distance between the main board and mezzanine boards is 10mm. While the prototype board is mounted using simple 10mm nickel-brass Hex spacers, a future design could accommodate a custom aluminium bracket to act as a thermal interface between the two boards.

4.3 Xilinx Ultrascale FPGA

This board implements a large Xilinx Ultrascale FPGA, in a 1517 ball-grid-array package. The board is available in two different configurations, mounting different FPGA devices with the same footprint:

- XCKU060-FFVA1517
- XCKU115-FLVA1517

The same footprint supports also the XCKU085-FLVA1517 FPGA but we do not manufacture the board using this device.

The *Xilinx Ultrascale FPGA* is a complex device with many modes of operation and features. For the details of the interfaces, operation and programming, refer to the dedicated Xilinx documentation.

The assignment of the FPGA Logic banks is represented in Figure 4.

For detailed information about the signal and pin assignment of the FPGA, refer to [RD1].

The pin assignment has been performed taking into account the constraints described in the Xilinx document ‘Radiation Tolerant Kintex UltraScaleXQRKU060 FPGA Data Sheet’ (DS882.pdf), which would allow this board to also be populated with the FPGA version in a CNA1509 package instead of the commercial FFVA1517 package.

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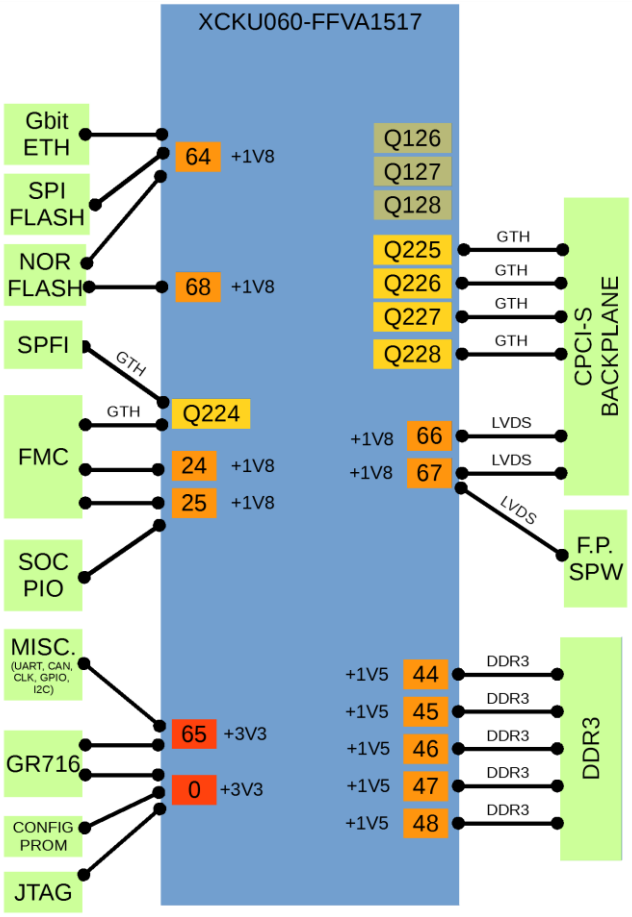

Figure 4 FPGA Bank and Signal Assignment

Bank 0 of the FPGA is the configuration and JTAG interface of the FPGA. To allow the GR716 to perform configuration of the FPGA via its SMAP interface, it must connect to the GR716 with 3.3V logic. This bank and Bank 65 are constrained to use an I/O voltage of 3.3V. Bank 65 is assigned also to the SMAP interface of the GR716 and for other miscellaneous 3.3V logic interface signals.

Logic banks 24 & 25 are assigned to the FMC-LPC interface (LVDS differential pairs) and to 1.8V logic for the PIO interface and are powered with an I/O voltage of 1.8V.

Logic banks 44, 45, 46, 47, 48 are dedicated to the 96 bit wide DDR3 Memory data interface and are powered with an I/O voltage of 1.5V. The pin assignment of these interfaces takes account of the assignment constraints imposed by the Xilinx 'Memory Interface Generator' (MIG) software for DDR3 interfaces.

Logic bank 64 is assigned to the Dual Gbit Ethernet interface, the SPI Data flash and the parallel NOR flash interface and is powered with an I/O voltage of 1.8V

Logic banks 66 and 67 are assigned to the SPW interfaces (LVDS differential pairs) and are powered with an I/O voltage of 1.8V

Logic bank 68 is also assigned to the parallel NOR flash interface and is powered with an I/O voltage of 1.8V.

GTH banks Q224 provides high speed transceiver links for the Front Panel SPFI interface and the optional High Speed serial link pins on the FMC connector.

GTH banks Q225, Q226, Q227, Q228 provide high speed transceiver links to the CPCI-S backplane.

Important note:

- GTH banks Q126, Q127, Q128 are unused on the version of the board mounting the XCKU060 FPGA .
- GTH banks Q126, Q127, Q128, Q229,Q230, Q231, Q232 on the version of the board mounting the XCKU115 FPGA.
- The GTH primitives corresponding to the unused GTH banks should not be instantiated or enabled in the FPGA design.

4.4 GR716 Microcontroller

The microcontroller has the following interfaces as represented in Figure 5.

SMAP	Parallel data interface for read-out and programming of FPGA configuration.
I2C	Two-wire Serial I2C interface with GR716 as Master (see section 4.6.6)
SPI	SPI master interface for user-defined SPI data exchange with FPGA
FPIO[3..0]	Four 3.3V LVTTL signals for user defined signalling between GR716 and FPGA
SPW	Spacewire LVDS interface between GR716 and FPGA
CAN3	CAN data interface between GR716 and Backplane
CAN4	CAN data interface between GR716 and Backplane
SPI-BOOT	SPI Memory interface to Serial SPI memory (see section 4.5)
SPI-DATA	SPI Memory interface to Serial SPI memory (see section 4.5)
UART2	2-wire Serial UART interface to GR716 UART0 interface
DSU	2-wire Serial UART interface to GR716 Debug Support Unit interface
GR-STS	GPIO output connected to front-panel LED for user defined signalling
GR-EN	Front panel DIP Switch connected to GR716 DSU Enable input
GR-BRE	Front panel DIP Switch connected to GR716 DSU Break input
GPIO-HDR28	GPIO signals for GR716 connected to standard 0.1” header for user defined purposes
FMC-ON	GPIO to Power Circuits to control the enabling of the +12V FMC power supply

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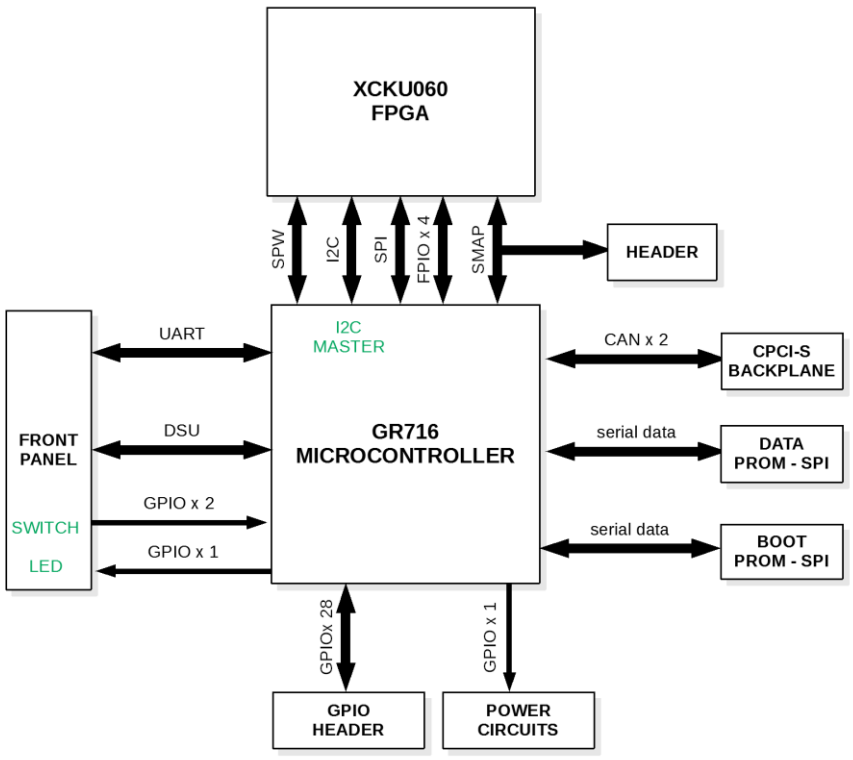

Figure 5 GR716 Interfaces

Table 1 Definition of GR716 GPIO pin functions

GR716 GPIO pin	Interface	Function
GPIO0	SPI Data Prom	SLV1
GPIO1	SPI Data Prom	SCK1
GPIO2	SPI Data Prom	MOSI1
GPIO3	SPI Data Prom	MISO1
GPIO4	GPIO to FPGA	FIO0
GPIO5	GPIO to FPGA	FIO1
GPIO6	GPIO to FPGA	FIO2
GPIO7	GPIO to FPGA	FIO3
GPIO8	GPIO to Power Control	FMC-ON
GPIO9	GPIO Header	GPIO9
GPIO10	GPIO Header	GPIO10
GPIO11	GPIO Header	GPIO11
GPIO12	GPIO Header	GPIO12
GPIO13	SPI to FGPA	SCLK0
GPIO14	SPI to FGPA	MISO0
GPIO15	SPI to FGPA	MOSI0
GPIO16	GPIO Header	GPIO16
GPIO17	SPI to FGPA	SLV0
GPIO18	GPIO Header	GPIO18
GPIO19	GPIO Header	GPIO19
GPIO20	GPIO Header	GPIO20
GPIO21	GPIO Header	GPIO21

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GR716 GPIO pin	Interface	Function
GPIO22	GPIO Header	GPIO22
GPIO23	GPIO Header	GPIO23
GPIO24	GPIO Header	GPIO24
GPIO25	SMAP to FPGA	SMAP_INITN
GPIO26	SMAP to FPGA	SMAP_DONE
GPIO27	SMAP to FPGA	SMAP_D0
GPIO28	SMAP to FPGA	SMAP_D1
GPIO29	SMAP to FPGA	SMAP_D2
GPIO30	SMAP to FPGA	SMAP_D3
GPIO31	SMAP to FPGA	SMAP_D4
GPIO32	SMAP to FPGA	SMAP_D5
GPIO33	SMAP to FPGA	SMAP_D6
GPIO34	SMAP to FPGA	SMAP_D7
GPIO35	SMAP to FPGA	SMAP_PROGN
GPIO36	SMAP to FPGA	SMAP_RDWR
GPIO37	SMAP to FPGA	SMAP_CSIN
GPIO38	SMAP to FPGA	SMAP_SCLK
GPIO39	GPIO Header	GPIO39
GPIO40	GPIO Header	GPIO40
GPIO41	I2C	SDA
GPIO42	I2C	SCL
GPIO43	GPIO Header	GPIO43
GPIO44	GPIO Header	GPIO44
GPIO45	GPIO Header	GPIO45
GPIO46	GPIO Header	GPIO46
GPIO47	GPIO Header	GPIO47
GPIO48	GPIO Header	GPIO48
GPIO49	GPIO Header	GPIO49
GPIO50	UART	RXD2
GPIO51	UART	TXD2
GPIO52	GPIO Header	GPIO52
GPIO53	GPIO Header	GPIO53
GPIO54	GPIO Header	GPIO54
GPIO55	GPIO Header	GPIO55
GPIO56	GPIO Header	GPIO56
GPIO57	Front Panel LED	GR-STS
GPIO58	CAN to backplane	CAN-TX3
GPIO59	CAN to backplane	CAN-RX3
GPIO60	GPIO Header	GPIO60
GPIO61	CAN	CAN-RX4
GPIO62	CAN	CAN-TX4
GPIO63	GPIO Header	GPIO63

The *GR716 microcontroller* is a complex device with many modes of operation. For the details of the interfaces, operation and programming, refer to [RD4].

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4.5 Memory

This boards incorporates various on-board memories as represented in Figure 6:

DDR3-SDRAM Dual SODIMM sockets for DDR3 SDRAM memory (96 bit wide interface). Nominally this data width can provide 64 bit data and 32 bit check-bit data for error correction. Due to constraints in the internal FGPA design, these are implemented with two controller interfaces.

FPGA-CONFIG 512 Mbit SPI memory (Cypress, S25FL512SAGN in SOIC-16 package) as non-volatile storage for the FPGA configuration.

FPGA-MEMORY 512 Mbit SPI memory (Cypress, S25FL512SAGN in SOIC-16 package) for FPGA non-volatile memory

NOR-FLASH Parallel Flash memory (40 bit wide) connected to FPGA, implemented using Cypress, Spansion, S29GL064S90TFVV10, 64 Mbit (8 M x 8-Bit/4M x 16-Bit), 1.8 V Flash PROM, in, TSOP-56 packages.

GR716-BOOT 512 Mbit SPI memory (Cypress, S25FL512SAGN in SOIC-16 package) for GR716-boot configuration

GR716-DATA 512 Mbit SPI memory (Cypress, S25FL512SAGN in SOIC-16 package) for GR716-data non-volatile memory

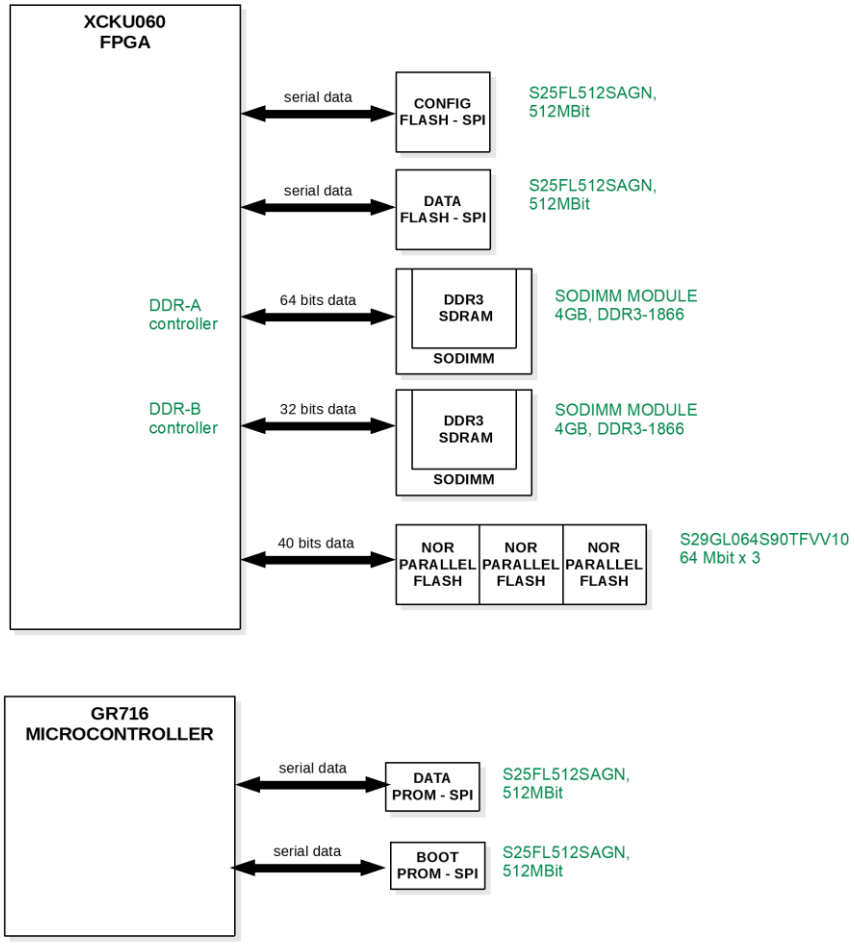

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Figure 6 Board Memory Configuration

4.6 Board Interfaces

4.6.1 High-Speed Serial Links

The board incorporates a large number of SPFI and SpaceWire Links distributed between the FPGA, CPCI-S backplane, GR716 Processor and External Front panel connectors as represented in Figure 7.

The Front panel Spacewire connections are buffered with *DS10BR150TSD/NOPB* LVDS transceivers.

The Front Panel SPFI connections are buffer with a *DS80PCI102SQ/NOPB* CML re-driver circuit.

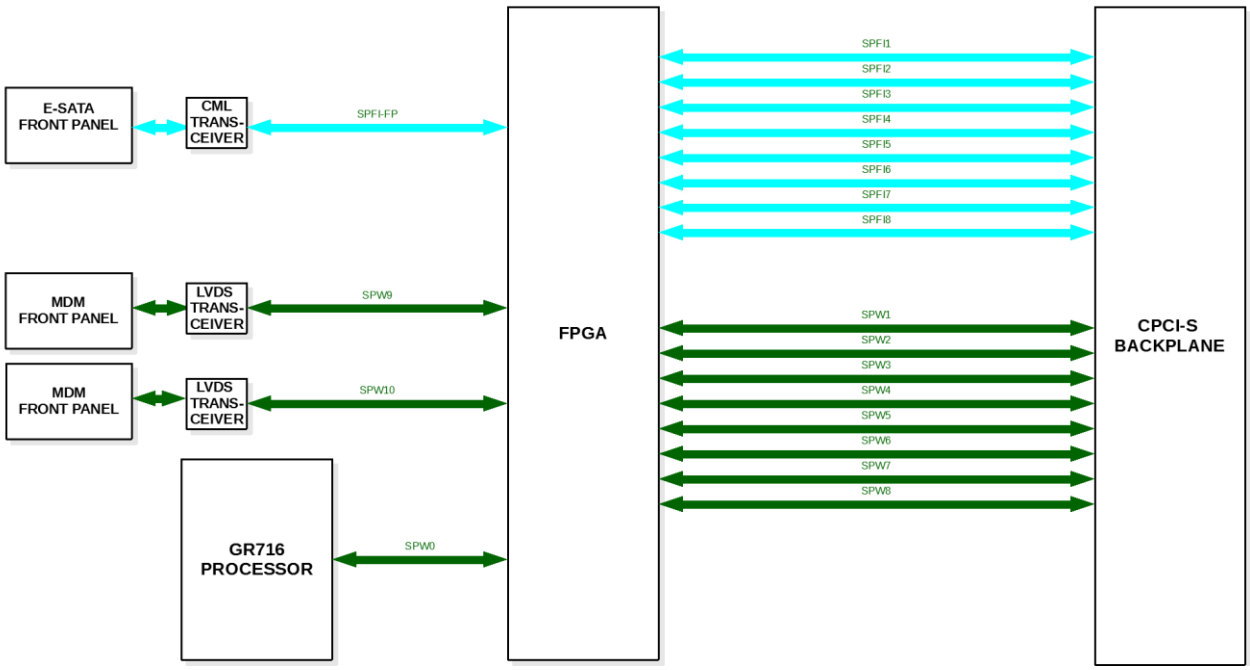

Figure 7 On-Board SpaceWire Connections

SPW links which connect to the FPGA are implemented using using the LVDS differential drivers/receivers implemented in the FPGA.

All SPW links which connect to the backplane (SPW1to SPW8) include resistors to provide Fail-safe/Cold-Spare protection network as shown in Figure 8. This means the internal 100Ohm differential pair termination inside the FPGA cannot be used for these links.

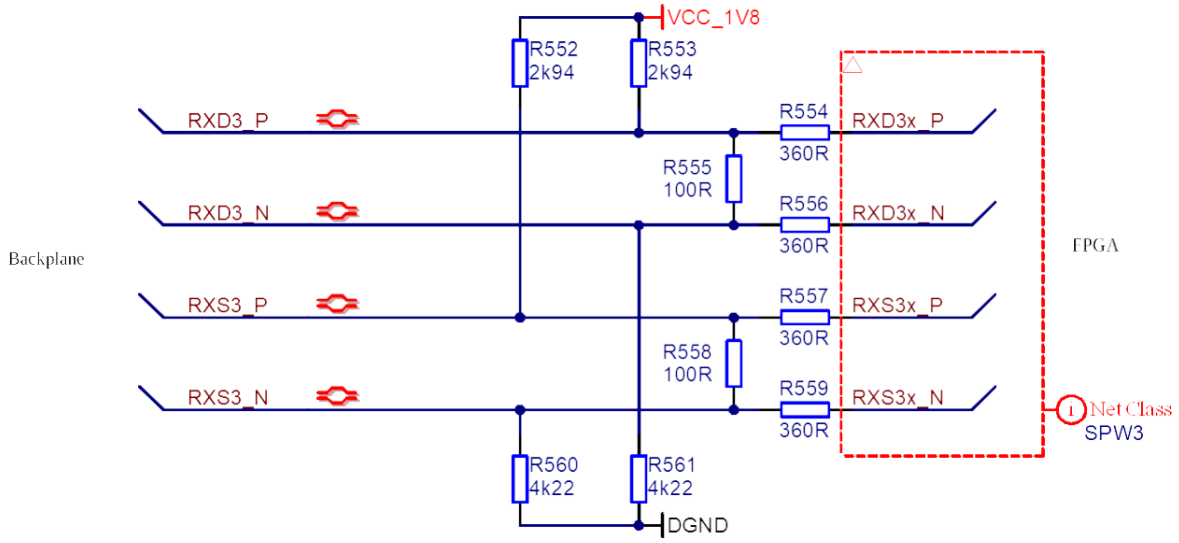

Figure 8 SPW fail-safe RX network

The interface signal to FPGA pin correspondence is listed in Table 2 .

Table 2 SPW Interface to FPGA pin mapping

Interface	Signal	FPGA Bank	FPGA Signal	FPGA pin
SPW0	TXD_N/_P	Bank 67	IO_L4	T17/T18
	TXS_N/_P	Bank 67	IO_L3	N16/N17
	RXD_N/_P	Bank 67	IO_L2	P16/R16
	RXS_N/_P	Bank 67	IO_L1	P18/P19
SPW1	TXD_N/_P	Bank 67	IO_L16	E17/F17
	TXS_N/_P	Bank 67	IO_L14	H17/H18
	RXD_N/_P	Bank 67	IO_L21	A19/B19
	RXS_N/_P	Bank 67	IO_L23	A20/B20
SPW2	TXD_N/_P	Bank 66	IO_L16	F12/F13
	TXS_N/_P	Bank 66	IO_L15	D14/D15
	RXD_N/_P	Bank 66	IO_L13	E15/F15
	RXS_N/_P	Bank 66	IO_L14	F14/G15
SPW3	TXD_N/_P	Bank 67	IO_L12	J18/K18
	TXS_N/_P	Bank 67	IO_L11	J19/J20
	RXD_N/_P	Bank 67	IO_L9	L18/L19
	RXS_N/_P	Bank 67	IO_L10	J16/K16
SPW4	TXD_N/_P	Bank 67	IO_L20	C18/D18
	TXS_N/_P	Bank 67	IO_L19	C19/D19

Interface	Signal	FPGA Bank	FPGA Signal	FPGA pin
	RXD_N/_P	Bank 67	IO_L13	G19/H19
	RXS_N/_P	Bank 67	IO_L15	F19/G20
SPW5	TXD_N/_P	Bank 67	IO_L23	B17/C17
	TXS_N/_P	Bank 67	IO_L24	A17/A18
	RXD_N/_P	Bank 67	IO_L17	E20/F20
	RXS_N/_P	Bank 67	IO_L18	E18/F18
SPW6	TXD_N/_P	Bank 66	IO_L12	H14/J14
	TXS_N/_P	Bank 66	IO_L11	G15/G16
	RXD_N/_P	Bank 66	IO_L10	J15/K15
	RXS_N/_P	Bank 66	IO_L9	K12/K13
SPW7	TXD_N/_P	Bank 66	IO_L19	A12/A13
	TXS_N/_P	Bank 66	IO_L20	C13/D13
	RXD_N/_P	Bank 66	IO_L18	E12/E13
	RXS_N/_P	Bank 66	IO_L17	D16/E16
SPW8	TXD_N/_P	Bank 66	IO_L7	H13/J13
	TXS_N/_P	Bank 66	IO_L8	L12/L13
	RXD_N/_P	Bank 66	IO_L5	L15/M15
	RXS_N/_P	Bank 66	IO_L6	P14/P15
SPW9	TXD_N/_P	Bank 67	IO_L8	M16/M17
	TXS_N/_P	Bank 67	IO_L7	K17/L17
	RXD_N/_P	Bank 67	IO_L6	R17/R18
	RXS_N/_P	Bank 67	IO_L5	N18/N19
SPW10	TXD_N/_P	Bank 66	IO_L24	B14/C14
	TXS_N/_P	Bank 66	IO_L21	A14/A15
	RXD_N/_P	Bank 66	IO_L23	B15/B16
	RXS_N/_P	Bank 66	IO_L22	B12/C12

SPFI links are implemented using using the GTH High Speed Transceivers of the FPGA. As per the SPFI requirements, all links are AC coupled and have 100kOhm pull-down resistors to ground.

The interface signal to FPGA pin correspondence is listed in Table 3 .

Table 3 SPFI Interface to FPGA pin mapping

Interface	Signal	FPGA Bank	FPGA Signal	FPGA pin
SPFI1	TXD1_P/_N	Bank 228	TX3	V6/V5
	RXD1_P/_N	Bank 228	RX3	V2/V1
	TXD2_P/_N	Bank 228	TX2	Y6/Y5
	RXD2_P/_N	Bank 228	RX2	W4/W3
SPFI2	TXD1_P/_N	Bank 228	TX1	AA4/AA3
	RXD1_P/_N	Bank 228	RX1	Y2/Y1
	TXD2_P/_N	Bank 228	TX0	AB6/AB5

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Interface	Signal	FPGA Bank	FPGA Signal	FPGA pin
	RXD2_P/_N	Bank 228	RX0	AB2/AB1
SPFI3	TXD1_P/_N	Bank 227	TX3	AD6/AD5
	RXD1_P/_N	Bank 227	RX3	AC4/AC3
	TXD2_P/_N	Bank 227	TX2	AE4/AE3
	RXD2_P/_N	Bank 227	RX2	AD2/AD1
SPFI4	TXD1_P/_N	Bank 227	TX1	AF6/AF5
	RXD1_P/_N	Bank 227	RX1	AF2/AF1
	TXD2_P/_N	Bank 227	TX0	AG8/AG7
	RXD2_P/_N	Bank 227	RX0	AG4/AG3
SPFI5	TXD1_P/_N	Bank 226	TX3	AH6/AH5
	RXD1_P/_N	Bank 226	RX3	AH2/AH1
	TXD2_P/_N	Bank 226	TX2	AJ8/AJ7
	RXD2_P/_N	Bank 226	RX2	AJ4/AJ3
SPFI6	TXD1_P/_N	Bank 226	TX1	AK6/AK5
	RXD1_P/_N	Bank 226	RX1	AK2/AK1
	TXD2_P/_N	Bank 226	TX0	AL8/AL7
	RXD2_P/_N	Bank 226	RX0	AL4/AL3
SPFI7	TXD1_P/_N	Bank 225	TX3	AM6/AM5
	RXD1_P/_N	Bank 225	RX3	AM2/AM1
	TXD2_P/_N	Bank 225	TX2	AN8/AN7
	RXD2_P/_N	Bank 225	RX2	AN4/AN3
SPFI8	TXD1_P/_N	Bank 225	TX1	AP6/AP5
	RXD1_P/_N	Bank 225	RX1	AP2/AP1
	TXD2_P/_N	Bank 225	TX0	AR8/AR7
	RXD2_P/_N	Bank 225	RX0	AR4/AR3
SPFI-FP	TXD_P/_N	Bank 224	TX3	AT6/AT5
	RXD_P/_N	Bank 224	RX3	AT2/AT1

4.6.2 Ethernet

A Dual Ethernet RJ45 interface is provided on the board front panel, and is connected to the FPGA. This interface can operate in either 100Mbit or Gbit mode, and can be used for standard networking.

Two external PHY devices, (*Micrel KSZ9031RNX*) are implemented on the board.

These PHY devices interface to the FPGA using the RGMII interface standard.

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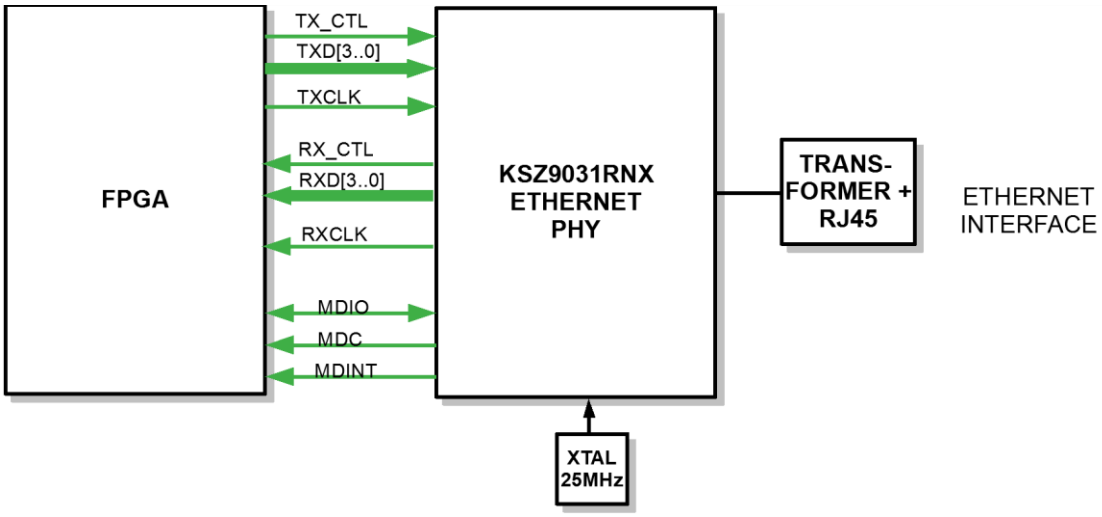

Figure 9 Ethernet RGMII to FPGA interface (1 of 2 shown)

Each interface has a separate MDIO interface connection to the FPGA.

The interface signal to FPGA pin correspondence is listed in Table 4 and Table 5 .

Table 4 ETH0 Interface to FPGA pin mapping

Interface	Signal	FPGA Bank	FPGA Signal	FPGA pin
ETH0	TXD0	Bank 64	IO_L12N	AN19
	TXD1	Bank 64	IO_L14N	AL18
	TXD2	Bank 64	IO_L11N	AN17
	TXD3	Bank 64	IO_L10N	AP18
	RXD0	Bank 64	IO_L16P	AK18
	RXD1	Bank 64	IO_L16N	AK17
	RXD2	Bank 64	IO_L15N	AK16
	RXD3	Bank 64	IO_L15P	AJ16
	TXCLK	Bank 64	IO_L12P	AM19
	TX_CTL	Bank 64	IO_L9N	AM19
	RXCLK	Bank 64	IO_L14P	Al19
	RX_CTL	Bank 64	IO_L9P	AP16
	MDINT	Bank 64	IO_T1U	AN16
	MDC	Bank 64	IO_L13N	AM17
	MDIO	Bank 64	IO_L10P	AP19

Table 5 ETH1 Interface to FPGA pin mapping

Interface	Signal	FPGA Bank	FPGA Signal	FPGA pin
ETH1	TXD0	Bank 64	IO_L6N	AU19
	TXD1	Bank 64	IO_L4P	AV19
	TXD2	Bank 64	IO_L5P	AT18
	TXD3	Bank 64	IO_L6P	AT19

Interface	Signal	FPGA Bank	FPGA Signal	FPGA pin
	RXD0	Bank 64	IO_L3P	AU17
	RXD1	Bank 64	IO_L5N	AT17
	RXD2	Bank 64	IO_L3N	AU16
	RXD3	Bank 64	IO_L7N	AR17
	TXCLK	Bank 64	IO_L11P	AN18
	TX_CTL	Bank 64	IO_L4N	AW18
	RXCLK	Bank 64	IO_L13P	AL17
	RX_CTL	Bank 64	IO_L7P	AR18
	MDINT	Bank 64	IO_L8P	AR20
	MDC	Bank 64	IO_T0U	AU20
	MDIO	Bank 64	IO_L8N	AT20

4.6.3 PPS

Two SMA connectors are provided on the front panel for user use and expected to be used for PPS inputs or outputs.

No detailed specification for the type or levels for these signals has been given.

These are therefore connected directly to the FPGA as LVTTL/LVCMOS33 signals, and care should be taken to ensure the allowable input voltage is not exceeded.

The interface signal to FPGA pin correspondence is listed in Table 6 .

Table 6 PPS Interface to FPGA pin mapping

Interface	Signal	FPGA Bank	FPGA Signal	FPGA pin
PPS	PPS0	Bank 65	IO_L13P	AL12
	PPS1	Bank 65	IO_L14P	AL14

4.6.4 FTDI (USB Serial)

An FTDI FT4232 serial to USB interface chip is implemented on the board to allow an external PC to interface to the following serial interfaces:

- *GR716* DSU serial interface
- *GR716* UART-0 serial interface
- *GR716* UART-1 serial interface
- FMC JTAG interface

The front panel interface connector (marked '*FTDI'* on the front panel) is a standard USB Micro-AB style connector.

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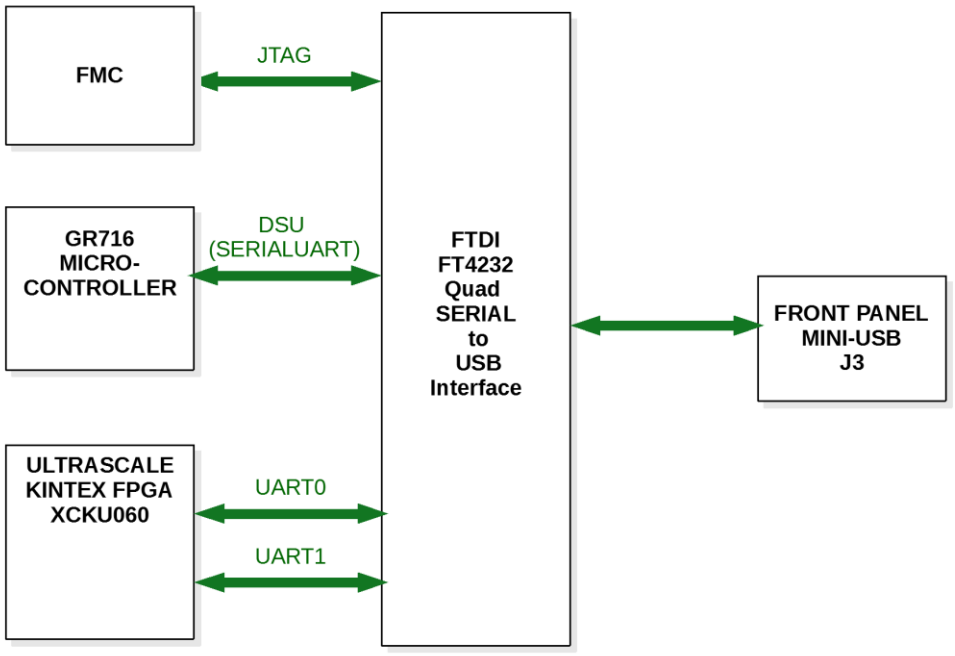

Figure 10 FTDI UART to Serial Interface

The interface signal to FPGA pin correspondence is listed inTable 7 .

Table 7 FTDI Interface to FPGA pin mapping

Interface	Signal	FPGA Bank	FPGA Signal	FPGA pin
UART0	TXD0	Bank 65	IO_L3P	AV13
	RXD0	Bank 65	IO_L3N	AW13
UART1	TXD1	Bank 65	IO_L9N	AT12
	RXD1	Bank 65	IO_L5N	AV12

The interface signal to GR716 interface pin correspondence is listed in Table 8 .

Table 8 FTDI Interface to GR716 pin mapping

Interface	Signal		GR716 Signal	GR716 pin
UART2	TXD2		GPIO50	65
	RXD2		GPIO51	66
DSU	DSUTX		DSUTX	8
	DSURX		DSURX	7

4.6.5 FMC Mezzanine Board Interface

The Mezzanine connector of the *GR-CPCI-S-BM-MEZZ* is a FMC High Pin Count (400 pin - Male) connector conforming to the VITA57.1 format. However, due to insufficient FPGA pins being available, not all of the HPC pins are populated.

The electrical functions connected over this interface are represented in the block diagram in Figure 11.

- *LA_P[33..0]/LA_N[33..0]* 34 LVDS differential pairs (configurable also as 68 single ended

1.8V LVCMOS signals). Functionality and configuration depend on the logic implemented in the FPGA and FMC mezzanine board.

- *CLK_C2M_P/_N* LVDS differential clock from Carrier (FPGA) to Mezzanine (FMC board)
- *CLK_M2C_P/_N* LVDS differential clock from Mezzanine (FMC board) to Carrier (FPGA)
- *PRSNTN* LVCMOS18 signal, pulled high to indicate to FPGA if FMC board is installed.
- *PWRGOOD* Signal from Mezzanine board indicating the 'Power Good' status of the circuits on the FMC board.
- *I2C* I2C slave signals connected from FMC board to GR716
- *DP_C2M_P/_N* High Speed serial TX pair from Carrier (FPGA) to Mezzanine (FMC)
- *DP_M2C_P/_N* High Speed serial TX pair from Mezzanine (FMC) to Carrier (FPGA)
- *GC_M2C_P/_N* Differential Clock from Mezzanine (FMC) to Carrier (FPGA)
- *JTAG* JTAG interface
- *Power*
    - 3V3P & 3V3PAUX 3.3V
    - VADJ 1.8V
    - +12V_FMC +12V. As per the system requirements, this supply voltage is switched ON/OFF under control of the FMC-ON output of the GR716.
    - VREF_A_M2C Vref output from mezzanine board to FPGA

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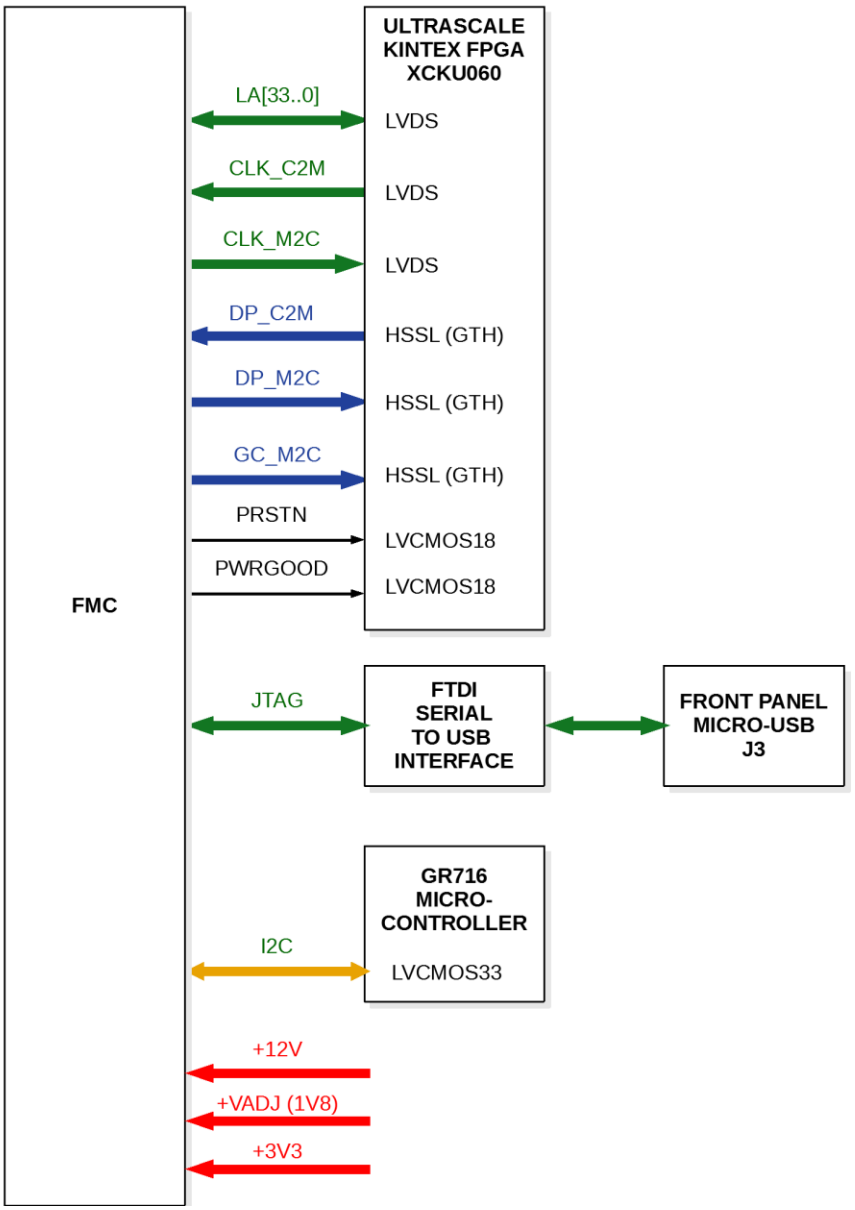

Figure 11 FMC Mezzanine Interface

With the exception of the *POWERGOOD* signal, all these signals are on the LPC section of the FMC connector.

The interface signal to FPGA pin correspondence is listed in Table 9 .

Table 9 FMC Interface to FPGA pin mapping

Interface	Signal	FPGA Bank	FPGA Signal	FPGA pin
FMC	CLK_C2M	Bank 24	IO_L10	AP29/AR30
	CLK_M2C	Bank 24	IO_L11	AM32/AN32
	LA00_P/_N	Bank 25	IO_L14	AN36/AN37
	LA01_P/_N	Bank 25	IO_L13	AP36/AR36
	LA02_P/_N	Bank 25	IO_L15	AN34/AP34

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Interface	Signal	FPGA Bank	FPGA Signal	FPGA pin
	LA03_P/_N	Bank 24	IO_L2	AV29/AW29
	LA04_P/_N	Bank 25	IO_L11	AR37/AT37
	LA05_P/_N	Bank 25	IO_L24	AL39/AM39
	LA06_P/_N	Bank 25	IO_L17	AM34/AM35
	LA07_P/_N	Bank 24	IO_L22	AH28/AJ28
	LA08_P/_N	Bank 25	IO_L9	AU37/AV37
	LA09_P/_N	Bank 25	IO_L21	AL34/AL35
	LA10_P/_N	Bank 25	IO_L23	AK35/AK36
	LA11_P/_N	Bank 25	IO_L12	AR38/AT38
	LA12_P/_N	Bank 24	IO_L5	AU31/AV31
	LA13_P/_N	Bank 25	IO_L18	AN39/AP39
	LA14_P/_N	Bank 25	IO_L19	AM36/AM37
	LA15_P/_N	Bank 24	IO_L12	AM31/AN31
	LA16_P/_N	Bank 25	IO_L10	AT39/AU39
	LA17_P/_N	Bank 24	IO_L13	AL30/AM30
	LA18_P/_N	Bank 24	IO_L14	AL29/AM29
	LA19_P/_N	Bank 24	IO_L4	AU29/AU30
	LA20_P/_N	Bank 24	IO_L3	AW30/AW31
	LA21_P/_N	Bank 24	IO_L6	AT29/AT30
	LA22_P/_N	Bank 24	IO_L7	AN33/AP33
	LA23_P/_N	Bank 24	IO_L17	AJ31/AK31
	LA24_P/_N	Bank 25	IO_L16	AN38/AP38
	LA25_P/_N	Bank 24	IO_L16	AK32/AL32
	LA26_P/_N	Bank 25	IO_L20	AL37/AL38
	LA27_P/_N	Bank 25	IO_L22	AK37/AK38
	LA28_P/_N	Bank 24	IO_L18	AJ33/AJ33
	LA29_P/_N	Bank 24	IO_L15	AJ30/AK30
	LA30_P/_N	Bank 24	IO_L19	AH29/AJ29
	LA31_P/_N	Bank 24	IO_L23	AF29/AG29
	LA32_P/_N	Bank 24	IO_L21	AE30/AF30
	LA33_P/_N	Bank 24	IO_L24	AE28/AF28
	PRSNTN	Bank 25	IO_T3U	AJ39
	PWRGOOD	Bank 25	IO_T2U	AP35
FMC-GBIT	DP_C2M	Bank 224	TX0_P/_N	AW8/AW7
	DP_M2C	Bank 224	RX0_P/_N	AW4/AW3
	GC_M2C	Bank 224	REFCLK0_P/_N	AT10/AT9

4.6.6 I2C

Two I2C chains are implemented in the design, as shown in Figure 12.

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1. A chain with GR716 as the Master, the FPGA, UCD9090 Power Sequencer and FMC board as Slaves. The Slave addresses of the FPGA and FMC board depend on the logic implemented in the design
2. A chain with FPGA as Master (if board is in a Host backplane slot) or as Slave (if the board is installed in a Peripheral backplane slot). The Slave addresses of the depend on the corresponding logic implemented.

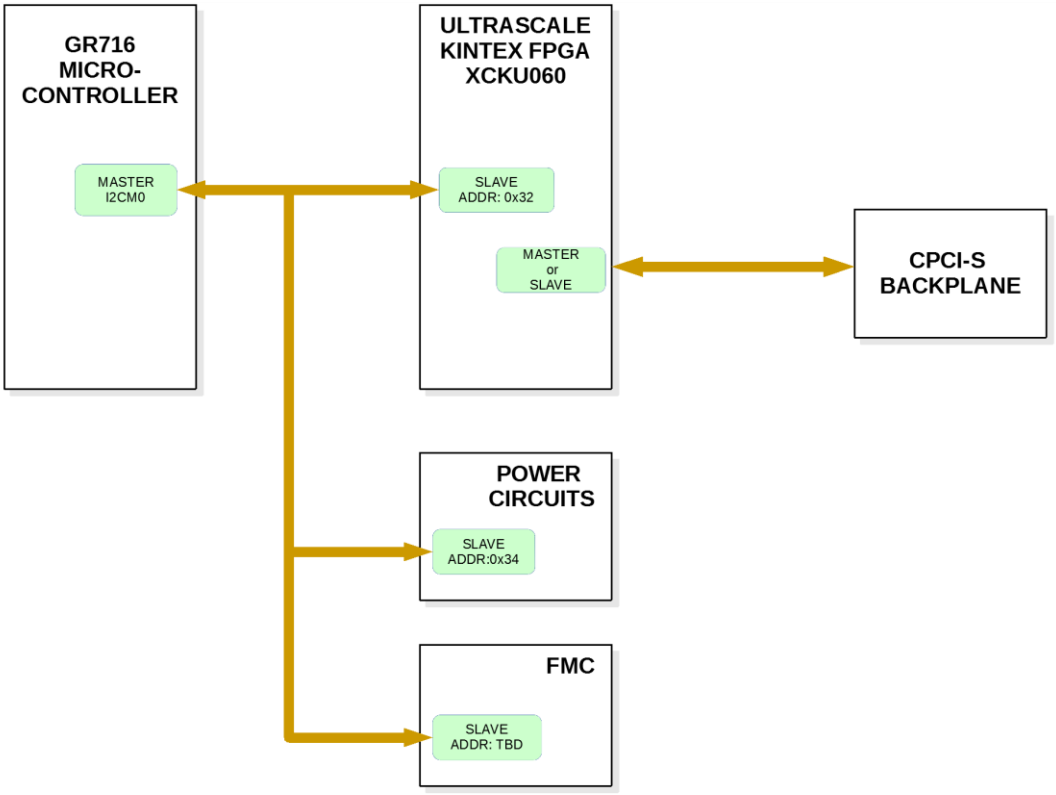

Figure 12 Board I2C Interfaces

4.6.7 JTAG

Two JTAG Chains are present in the designed:

1. JTAG1: This JTAG chain allows programming of the FPGA and its attached SPI Prom via a Digilent HS-2 JTAG module and dedicated front panel USB connector, J2 (marked '*FPGA-JTAG'* on the front panel). The JTAG signals are also available on a 14 pin header J14.
2. JTAG2: This JTAG chain connects to the JTAG signals of the FMC Mezzanine expansion connector via a FTDI USB to Serial Converter IC (section 4.6.4) and dedicated front panel USB connector, J3 (marked '*FTDI'* on the front panel).

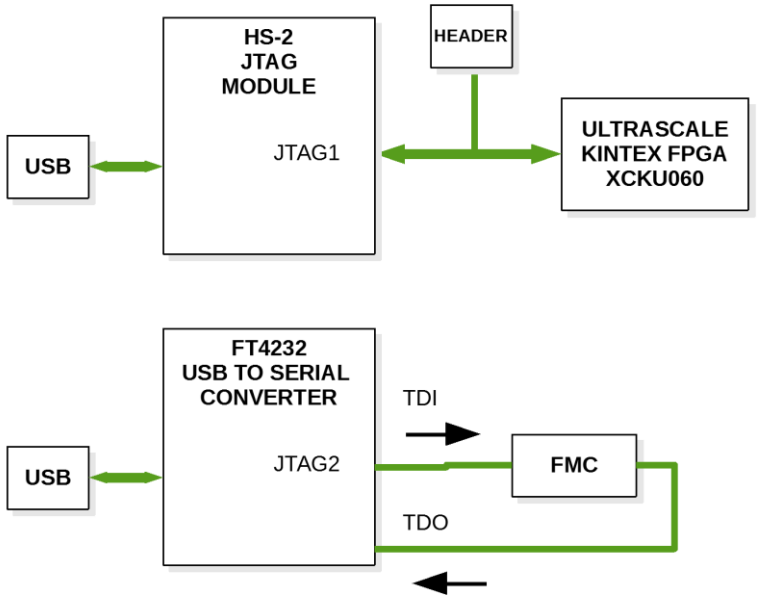

Figure 13 FPGA JTAG Interface

4.6.8 FPGA-GPIO

16 GPIO signals (SOCPIO[15..0]) are connected from the FPGA to a 20 pin header, *J9*.

This allows accessory boards to be easily attached to the board with a short ribbon cable, to provide additional IO functions. For example, connecting a *GR-ACC-6U-6UART* could provide 6 standard serial UART interface, or a *GR-ACC-GR740* board could provide 2 UART, 2 CAN and a Dual 1553 interface, if the logic in the FPGA is appropriately configured.

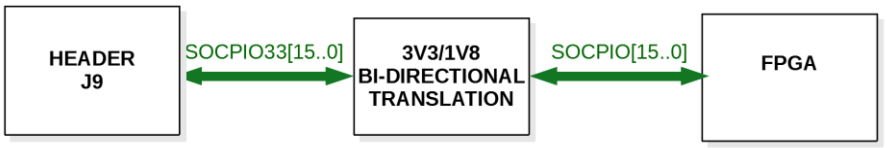

Figure 14 FPGA-GPIO interface

These FPGA signals are LVCMOS18 voltage levels but in order to ensure compatibility with accessory boards, 3V3 to1V8 translation buffers are included in the design. These Bi-directional buffers exhibit an output impedance of about 4kOhm which may limit the achievable drive strength.

The interface signal to FPGA pin correspondence is listed in Table 10 .

Table 10 FPGA-GPIO (SOC_PIO) Interface to FPGA pin mapping

Interface	Signal	FPGA Bank	FPGA Signal	FPGA pin
FPGA-GPIO	SOCPIO0	Bank 25	IO_L8P	AV38
	SOCPIO1	Bank 25	IO_L4N	AW26
	SOCPIO2	Bank 25	IO_L6N	AU35

Interface	Signal	FPGA Bank	FPGA Signal	FPGA pin
	SOCPIO3	Bank 25	IO_L7N	AV36
	SOCPIO4	Bank 25	IO_L5P	AR33
	SOCPIO5	Bank 25	IO_L7P	AU36
	SOCPIO6	Bank 25	IO_T0U	AR35
	SOCPIO7	Bank 25	IO_L5N	AT33
	SOCPIO8	Bank 25	IO_L2P	AV33
	SOCPIO9	Bank 25	IO_L3P	AT34
	SOCPIO10	Bank 25	IO_L1P	AW36
	SOCPIO11	Bank 25	IO_L6P	AT35
	SOCPIO12	Bank 25	IO_L3N	AU34
	SOCPIO13	Bank 25	IO_L4P	AW35
	SOCPIO14	Bank 25	IO_L2N	AV34
	SOCPIO15	Bank 25	IO_L1N	AW34

4.6.9 Reset Circuit

Two reset circuits are provided, each with a *TPS3705-33* processor supervisory circuit, which ensures that the reset is only released once the 3.3V power supply is within its normal limits, and that the reset pulse period has a well-defined period.

Additionally, the Reset signal for the *GR716* (*RST_GR716_N*) can be reset by the Backplane, or the Front Panel reset button.

The Reset signal for the *FPGA(SOC)* and *Ethernet PHY's* (*RST_SOC_N*) is derived from *RST_GR716_N,* but can additionally be reset by the Watchdog (*WDOGN*) output of the GR716.

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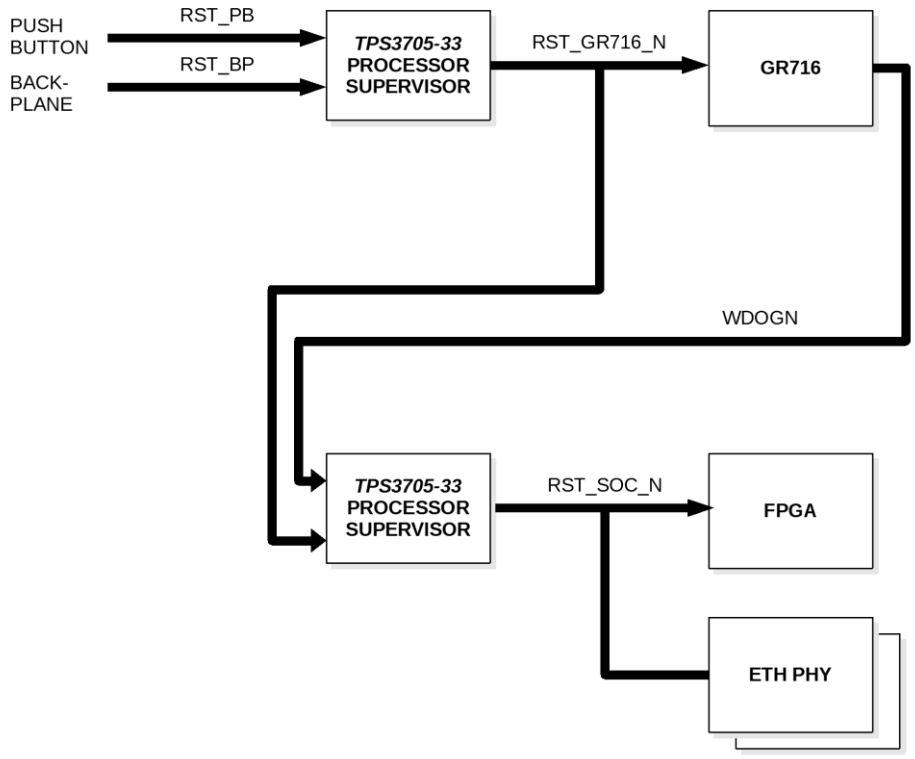

Figure 15 Reset Circuitry

4.6.10 CPCI-S Backplane

The CPCI-S Backplane interface is represented in Figure 16.

In the standard configuration the P0 and P3 connectors of the backplane are not used, and not installed on the board.

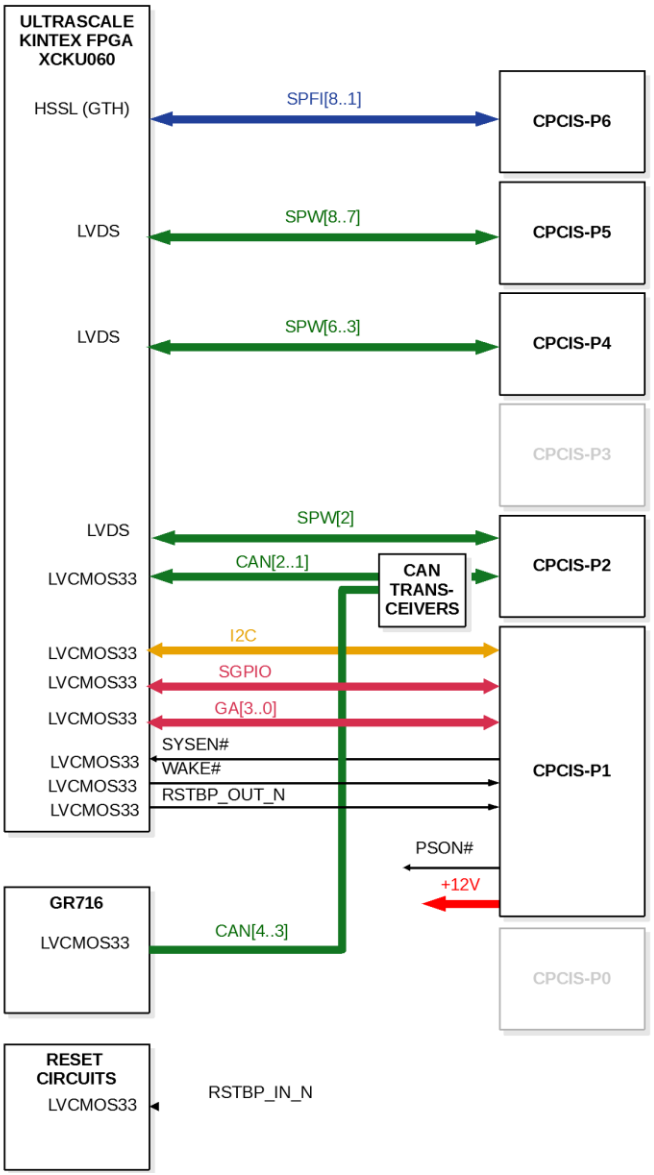

Figure 16 CPCI-S Interface

8 High-Speed Serial Links (HSSL) connect from the GTH transceiver interfaces of the FPGA to the P6 connector of the backplane.

8 Spacewire (SPW) links connect from LVDS interfaces of the FPGA to the P5, P4 and P2 connectors of the backplane.

2 CAN interfaces connect from the FPGA and 2 from the GR716 to the P1 connector of the backplane.

+12V power and a PSON# control signal are provided by the P1 connector of the backplane.

The interface signal to FPGA pin correspondence is listed in Table 11 .

The interface signal to GR716 pin correspondence is listed in Table 12 .

Table 11 Backplane Interface to FPGA pin mapping

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Interface	Signal	FPGA Bank	FPGA Signal	FPGA pin
SPFI[8..1]	See Table 3			
SPW[8..2]	See Table 2			
I2CBP	I2C_SDA2	Bank65	IO_L16N	AK15
	I2C_SCL2	Bank65	IO_L16P	AJ15
CAN1	TX1	Bank65	IO_L13N	AM12
	RX1	Bank65	IO_L11N	AN12
CAN2	TX2	Bank65	IO_L18P	AK13
	RX2	Bank65	IO_L14N	Al13
SGPIO	SDI	Bank65	IO_L24N	AD13
	SDO	Bank65	IO_L15N	AJ14
	SCL	Bank65	IO_L15P	AH14
	SL	Bank65	IO_T3U	AE15
GA	GA3	Bank65	IO_L19N	AH12
	GA2	Bank65	IO_L19P	AG12
	GA1	Bank65	IO_L18N	AK12
	GA0	Bank65	IO_L17P	AH13
System	SYSEN#	Bank65	IO_L17N	AJ13
	WAKE#	Bank65	IO_L20P	AF15
	RSTBP_OUT_N	Bank65	IO_L24P	AD14

Table 12 Backplane Interface to GR716 pin mapping

Interface	Signal		GR716 Signal	GR716 pin
CAN3	TX3		GPIO58	73
	RX3		GPIO59	74
CAN4	TX4		GPIO62	80
	RX4		GPIO61	79

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4.7 Oscillators and Clock Inputs

The oscillator and clock scheme for the *GR-CPCIS-XCKU Board* Board is shown in Figure 17. On this board, all oscillators are soldered to the PCB, except for X3 which is an 8 pin DIL socket for a user defined oscillator.

X1 provides a 20MHz oscillator input for the GR716 main input clock

X2 provides a 50MHzoscillator input for the GR716 Spacewire clock

Y1 is not fitted, but could be used as a Crystal for the internal GR716 oscillator.

X3 is a DIL8 socket for a user defined oscillator input to the FPGA

X4 is a 300MHz LVDS differential clock input to the FPGA. This clock is used internally by the FPGA to generate the Clocks for the DDR3 memory interface.

X5 is a 156.25MHz LVDS differential clock input to the FPGA. This clock is used internally by the FPGA to generate the Clocks for the GTH high speed serial transceivers.

Y2 is a 12.00 MHz crystal input for the FTDI USB/Serial interface chip

Y3 & Y4 are 25.00 MHz crystal inputs for the ETH0 and ETH1 Ethernet PHY chips respectively. The F1_GC_CLK, F1_CLK_M2C and F1_CLK_C2M are clock interfaces routed between the FPGA and FMC connector for possible future use, depending on the FPGA and FMC board logic requirements.

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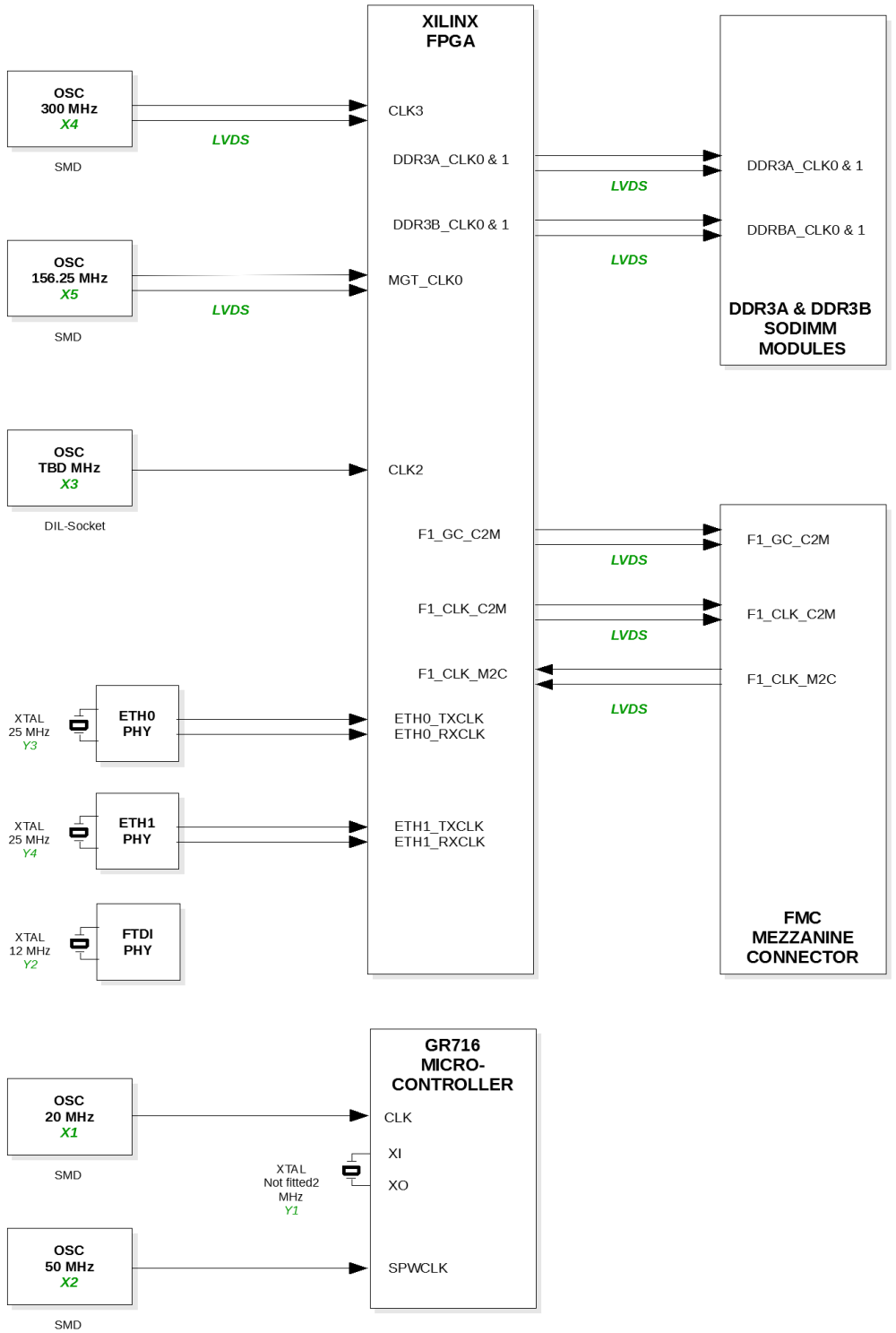

Figure 17 Board level Clock Distribution Scheme – GR-CPCIS-XCKU

4.8 Power Supply and Voltage Regulation

The power configuration scheme implemented on the *GR-CPCIS-XCKU* board is represented in Figure 18.

Power at a nominal input voltage of +12V can be provided from the CPCI-S connections of the backplane, or in stand-alone mode

- for S/N 001, 002, and 003 from a dedicated 2-pin connector on the board (J18);
- for others S/N from a power jack SMD connector (J18)

For the board, the nominal supply input is considered to be +12V via the backplane, but in stand alone operation it can also be powered:

- [for S/N 001, 002, 003] from a +12V bench supply;
- [for others S/N] from the 12V power supply included in the delivery kit.

The maximum limit is +14.5V due to the 15V transient protection diode at the input.

As per the CPCI-S specification an active low external signal PS_ON# must be driven in order to enable a power switch on the board and allow the local circuits to be powered up.

In a stand-alone board configuration the slide switch S4 performs the control of the PS_ON# signal.

On-board DCDC buck and Linear regulators provide the various voltage required by the rest of the circuits on the board, as schematically represented in Figure 18.

VCC_0V95 FPGA Vcore and BRAM supply voltages

PM_3V3 Dedicated 3.3V supply for Power Monitor circuit

VCC_3V3 +3.3V supply for VIO for FPGA, GR716 and peripherals

VCC_1V8 +1V8 supply for VIO for FPGA, GR716 and peripherals

VCC_1V5 +1V5 supply for VIO for FPGA, and DDR3 memory circuits

ETH_1V2 +1V2 supply for Ethernet PHY circuits

GTH_1V0 Linear regulated 1.0V supply for FPGA Gigabit Transceivers

GTH_1V2 Linear regulated 1.2V supply for FPGA Gigabit Transceivers

GTH_1V8 Linear regulated 1.8V supply for FPGA Gigabit Transceivers

VTTVREF Linear regulated 0.75V supply for DDR3 reference voltage

VTTVREF2 Linear regulated 0.75V supply for DDR3 reference voltage

VTTVDDR Linear regulated 0.75V supply for DDR3 termination voltage

VTTVDDR2 Linear regulated 0.75V supply for DDR3 termination voltage

Since the FPGA has specific power up and sequencing requirements this board implements a voltage monitoring and sequencing circuit using a *UCD9090*, 10-Channel Sequencer and System Health Monitor circuit.

This circuit is pre-programmed via its PM-BUS (I2C) interface to perform the required start-up and shut-down power sequencing.

The voltages and currents which the device monitors are indicated via ‘V’ and ‘A’ in Figure 18. These voltages/current values can be read-out from the *UCD9090* via the I2C interface which is connected to the GR716.

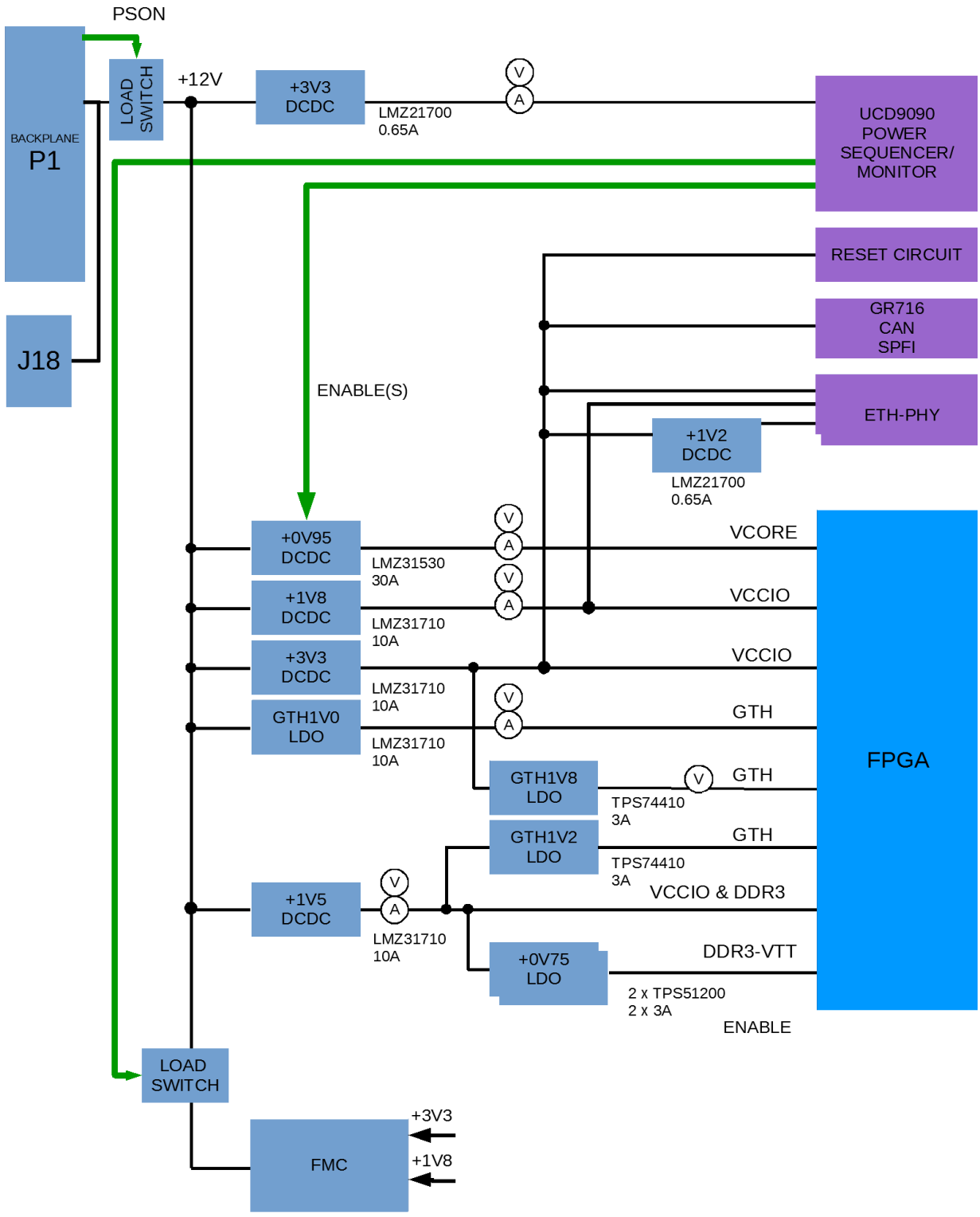

Figure 18 Power Regulation Scheme – GR-CPCIS-XCKU

5 SETTING UP AND USING THE BOARD

The board is provided with a default configuration set by bootstrap settings which may have to be changed to suit the User's preferences.

For additional information, refer to [RD1] and [RD4]. For information about the Bootstrap signals, refer to section 5.3.

To operate the board stand alone on the bench top, install the power configuration jumpers appropriately, and a power supply of +12V nominal to the board connector J18.

ATTENTION! To prevent damage to board, please ensure that the correct power supply voltage and polarity is used with the board.

Do not exceed +14.5V at the power supply input, as this may damage the board.

The PWR LED on the front panel should be illuminated indicating that the power supply is present and the board is generating the supply voltages that it requires.

5.1 GR716 Processor Programing and Debug

To perform program download and software debugging on the GR716 processor it is necessary to use the *Frontgrade Gaisler GRMON3* debugging software, installed on a host PC. Please refer to the GRMON3 documentation for the installation of the software on the host PC (Linux or Windows), and for the installation of the associated hardware dongle.

To perform software download and debugging on the processor, a link from the Host computer to the DSU interface of the board is necessary. As described in section 4.6.4 this is achieved via the FTDI USB interface.

Program download and debugging can be performed in the usual manner with GRMON3. More information on the usage, commands and debugging features of GRMON3, is given in the GRMON3 Users Manuals and associated documentation, [RD3].

5.2 FPGA Programing and Debug

Loading and programming of the FPGA configuration files is performed using the JTAG interface of the FPGA.This is accessed via the front panel J2 (marked '*FPGA-JTAG'* on the front panel) connector with a standard Micro-USB cable connected to a host computer running the Xilinx Vivado design software.

Please refer to the Xilinx Ultrascale and Vivado design software documentation for more information of the programming process.

5.3 Switches and Bootstrap Signals

A number of features of the board have configuration options which need to be set correctly in order for the board to operate correctly.

This includes:

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- GR716 Bootstrap signals / refer to [RD4] for detailed explanation of functions
- FPGA configuration options / refer to configuration documentation for Xilinx Ultrascale FPGA's
- Backplane interface pull-ups / refer to the Schematics, [RD1]

These signals and their meaning are listed below, together with the suggested default configuration.

Table 13 Board Default Jumper Settings

Jumper	Function	Type	Default
JP1	GR716 GPIO0 Disable EDAC	3 pin header	Pull-up: Install 1-2
JP2	GR716 GPIO17 Bypass InternalBoot PROM	3 pin header	Pull-Down: Install 2-3
JP3	GR716 GPIO62 Enable memory Test	3 pin header	Pull-Down: Install 2-3
JP4	GR716 GPIO63 Redundant memory available	3 pin header	Pull-Down: Install 2-3
JP5	GR716 DSUTX Copy ASW image	3 pin header	Pull-Down: Install 2-3
JP6	GR716 SPIM-MOSI Remote access/Boot from memory	3 pin header	Pull-Down: Install 2-3
JP7	GR716 SPIM_SCK Boot source 0	3 pin header	Pull-Down: Install 2-3
JP8	GR716 SPIM_Sel Boot source 1	3 pin header	Pull-Down: Install 2-3
JP9	FPGA MODE[2..0] Sets FPGA configuration mode pins	2x3pin header	Set Master SPI mode to automatically load configuration from SPI prom if this has been previously programmed. => "001" 1-2 Closed & 3-4, 5-6 Open
JP10	SMAP PULL-Ups 1-2 apply pull-down for SDRSTN 3-4 apply pull-up for SDCS 5-6 apply pull-up for SD3 7-8 apply pull-up for SD2	2x4pin header	1-2: Open 3-4: Closed 5-6: Closed 7-8: Closed
JP11	Backplane I2C 1-2 apply pull-up for SCL 3-4 apply pull-up for SDA 5-6 connect SCLto backplane 7-8 connect SDA to backplane	2x4pin header	1-2, 3-4, 5-6, 7-8: Closed
JP12	Backplane SGPIO 1-2 apply pull-up forSDI 3-4 apply pull-up for SDO 5-6 apply pull-up for SCL 7-8 apply pull-up for SL	2x4pin header	1-2, 3-4, 5-6, 7-8: Closed
JP13	FTDI Port A Install the jumpers to connect the JTAG interface from the FMC to the FTDI serial interface circuit	2x4pin header	1-2, 3-4, 5-6, 7-8: Closed
JP14	FTDI Port B Install the jumpers to connect the DSU UARTinterface from the GR716 FTDI serial interface circuit	2x4pin header	1-2, 3-4 closed 5-6, 7-8: don't-care

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Jumper	Function	Type	Default
JP15	FTDI Port C Install the jumpers to connect the UART interface from the FPGAto the FTDI serial interface circuit	2x4pin header	1-2, 3-4, 5-6, 7-8: Closed
JP16	SOCPIO33_0 Connects either SOCPIO0 signal from FPGA or UART RXD from the GR716 to connector J9 pin 1	3 pin header	Install 1-2; connects FPGA SOCPIO0 to HDR
JP17	SOCPIO33_1 Connects either SOCPIO1 signal from FPGA or UART TXD from the GR716 to connector J9 pin 2	3 pin header	Install 1-2; connects FPGA SOCPIO1 to HDR
JP18	WD Reset Install jumper to prevent Watchdog resetting system (e.g. during SW development).	2 pin header	1-2 open When GR716 is not mounted, connect J18 using the jumper. When jumper J18 not inserted FPGA/SOC and ETH0/ETH1 PHY's will be pulled to reset.

6 INTERFACES AND CONFIGURATION

6.1 List of Connectors

FRONT PANEL CONNECTORS

Table 14 List of Connectors – GR-CPCIS-XCKU / Front Panel

Name	Function	Type	Description
J1a	ETH-0	RJ45	GB Ethernet Connector
J1b	ETH-2	RJ45	GB Ethernet Connector
J2	JTAG-USB		Digilent HS-2 JTAG interface
J3	FTDI-Serial	Micro-USB	FTDI USB to serial interface – JTAG & UART
J4	PPS-0	SMB	Pulse-Per-Second Input - 0
J5	PPS-1	SMB	Pulse-Per-Second Input - 1
J6	SPFI	E-SATA	Spacefibre Interface 0 (to FGPA)
J7	SPW-0	MDM9S	Spacewire Interface 0 (to FGPA)
J8	SPW-1	MDM9S	Spacewire Interface 1 (to FGPA)

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ON BOARD HEADERS/CONNECTORS

Table 15 List of Connectors – GR-CPCIS-XCKU / On-Board

Name	Function	Type	Description
J9	FPGA-SOCPIO	HDR2X10pin 0.1”	SOCPIO interface to FPGA (for GR-ACC-6U-6UART)
J10	GR716-SOCPIO0	HDR2X10pin 0.1”	SOCPIO interface to GR716
J11	GR716-SOCPIO1	HDR2X10pin 0.1”	SOCPIO interface to GR716
J12	SODIMM-A	DDR3 204pin SODIMM	DDR3 Interface A (64 bits)
J13	SODIMM-B	DDR3 204pin SODIMM	DDR3 Interface B (32 bits)
J14	JTAG-FPGA	MOLEX 14pin_2mm	JTAG interface to FPGA
J15	PMBUS	HDR2X5_0.1”	PM bus interface to UCD9090 controller
J16	SDBUS	HDR2X4_0.1”	Header for Backplane SDBUS
J17	FAN	MOLEX_6410_3pin	Header for FPGA Fan (+12V)
J18	POWER	• [For S/N 001, 002, 003] MOLEX_0428192223_2pin • [For other S/N]: Power Jack, PJ-002A 2.1mm SMD	Connector for +12V power input
J19	SMAP1	HDR2X8pin 0.1”	Header for SMAP interface
J20	SMAP2	HDR2X8pin 0.1”	Header for SMAP interface

MEZZANINE

Table 16 List of Connectors – GR-CPCIS-XCKU / Mezzanine

Name	Function	Type	Description
FMC1	Mezzanine	FMC-HPC-400 pin	Mezzanine interface

BACKPLANE

Table 17 *List of Connectors – GR-CPCIS-XCKU / Backplane*

Name	Function	Type	Description
P0	CPCI-S Backplane	TE 10052825-101LF, Plug	CPCI-S Backplane Connector, 72 pos.
P1	CPCI-S Backplane	TE 10052825-101LF, Plug	CPCI-S Backplane Connector , 72 pos.
P2	CPCI-S Backplane	TE 10052837-101LF, Plug	CPCI-S Backplane Connector , 96 pos
P3	CPCI-S Backplane	TE 10052837-101LF, Plug	CPCI-S Backplane Connector , 96 pos
P4	CPCI-S Backplane	TE 10052837-101LF, Plug	CPCI-S Backplane Connector , 96 pos
P5	CPCI-S Backplane	TE 10052824-101LF, Plug	CPCI-S Backplane Connector , 96 pos
P6	CPCI-S Backplane	TE 10052838-101LF, Plug	CPCI-S Backplane Connector , 96 pos

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Figure 19 Front Panel View

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Pin	Name	Comment
1	TPFOP	Output +ve
2	TPFON	Output -ve
3	TPFIP	Input +ve
4	TPFOC	Output centre-tap
5		No connect
6	TPFIN	Input -ve
7	TPFIC	Input centre-tap
8		No connect

Table 1: J1a RJ45-ETHERNET Connector

Table 18 J1b RJ45-ETHERNET Connector

Pin	Name	Comment
1	TPFOP	Output +ve
2	TPFON	Output -ve
3	TPFIP	Input +ve
4	TPFOC	Output centre-tap
5		No connect
6	TPFIN	Input -ve
7	TPFIC	Input centre-tap
8		No connect

Table 19 J1 USB Micro connector – Digilent SMT2 JTAG

Pin	Name	Comment
1	VBUS	+5V (from external host)
2	DM	Data Minus
3	DP	Data Plus
4	ID	Not used
5	DGND	Ground

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Table 20 J3 USB Micro connector – FTDI Quad Serial Link

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Pin	Name	Comment
1	VBUS	+5V (from external host)
2	DM	Data Minus
3	DP	Data Plus
4	ID	Not used
5	DGND	Ground

Table 21 J4 PPS-0 Input

Pin	Name	Comment
INNER	+IN	Inner Pin, Pulse Per Second ,+3V3 logic
OUTER	DGND	Outer Pin Return

Table 22 J5 PPS-1 Input

Pin	Name	Comment
INNER	+IN	Inner Pin, Pulse Per Second ,+3V3 logic
OUTER	DGND	Outer Pin Return

Table 23 J6 Spacefibre Interface 0 (to FGPA)

Pin	Name	Comment
1	**DGND**	Ground
2	TX_DATA_P	Data In -ve
3	TX_DATA_N	Strobe In +ve
4	**DGND**	Ground
5	RX_DATA_P	Strobe In -ve
6	RX_DATA_N	Inner Shield
7	**DGND**	Ground

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Table 24 J7 SPW-0 interface connections (to FPGA)

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Pin	Name	Comment
1	DIN0+	Data In +ve
6	DIN0-	Data In -ve
2	SIN0+	Strobe In +ve
7	SIN0-	Strobe In -ve
3	SHIELD	Inner Shield
8	SOUT0+	Strobe Out +ve
4	SOUT0-	Strobe Out -ve
9	DOUT0+	Data Out +ve
5	DOUT0-	Data Out -ve

Table 25 J7 SPW-1 interface connections (to FPGA)

Pin	Name	Comment
1	DIN0+	Data In +ve
6	DIN0-	Data In -ve
2	SIN1+	Strobe In +ve
7	SIN1-	Strobe In -ve
3	SHIELD	Inner Shield
8	SOUT1+	Strobe Out +ve
4	SOUT1-	Strobe Out -ve
9	DOUT1+	Data Out +ve
5	DOUT1-	Data Out -ve

Table 26 J9 SOCPIO interface to FPGA (3V3 logic)

FUNCTION	CONNECTOR PIN			FUNCTION
SOCPIO0	1	■	2	SOCPIO1
SOCPIO2	3	□	4	SOCPIO3
SOCPIO4	5	□	6	SOCPIO5
SOCPIO6	7	□	8	SOCPIO7
SOCPIO8	9	□	10	SOCPIO9
SOCPIO10	11	□	12	SOCPIO11
SOCPIO12	13	□	14	SOCPIO13
SOCPIO14	15	□	16	SOCPIO15
VCC_3V3	17	□	18	VCC_3V3
DGND	19	□	20	DGND

Table 27 J10 GPIO interface to GR716 / 1 (3V3 logic)

FUNCTION	CONNECTOR PIN			FUNCTION
GPIO9	1	■	2	GPIO10
GPIO11	3	□	4	GPIO12
GPIO16	5	□	6	GPIO1/
GPIO19	7	□	8	GPIO20
GPIO21	9	□	10	GPIO22
GPIO23	11	□	12	GPIO24
GPIO39	13	□	14	GPIO40
GPIO43	15	□	16	GPIO44
VCC_3V3	17	□	18	VCC_3V3
DGND	19	□	20	DGND

Table 28 J11 GPIO interface to GR716 / 2 (3V3 logic)

FUNCTION	CONNECTOR PIN			FUNCTION
GPIO45	1	■	2	GPIO46
GPIO47	3	□	4	GPIO48
GPIO49	5	□	6	GPIO52
GPIO53	7	□	8	GPIO54
GPIO55	9	□	10	GPIO56
GPIO60	11	□	12	GPIO63
nc	13	□	14	nc
nc	15	□	16	nc
VCC_3V3	17	□	18	VCC_3V3
DGND	19	□	20	DGND

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Table 29 J12 - DDR3 204pin SODIMM - DDR3 Interface A:Data[63..0]

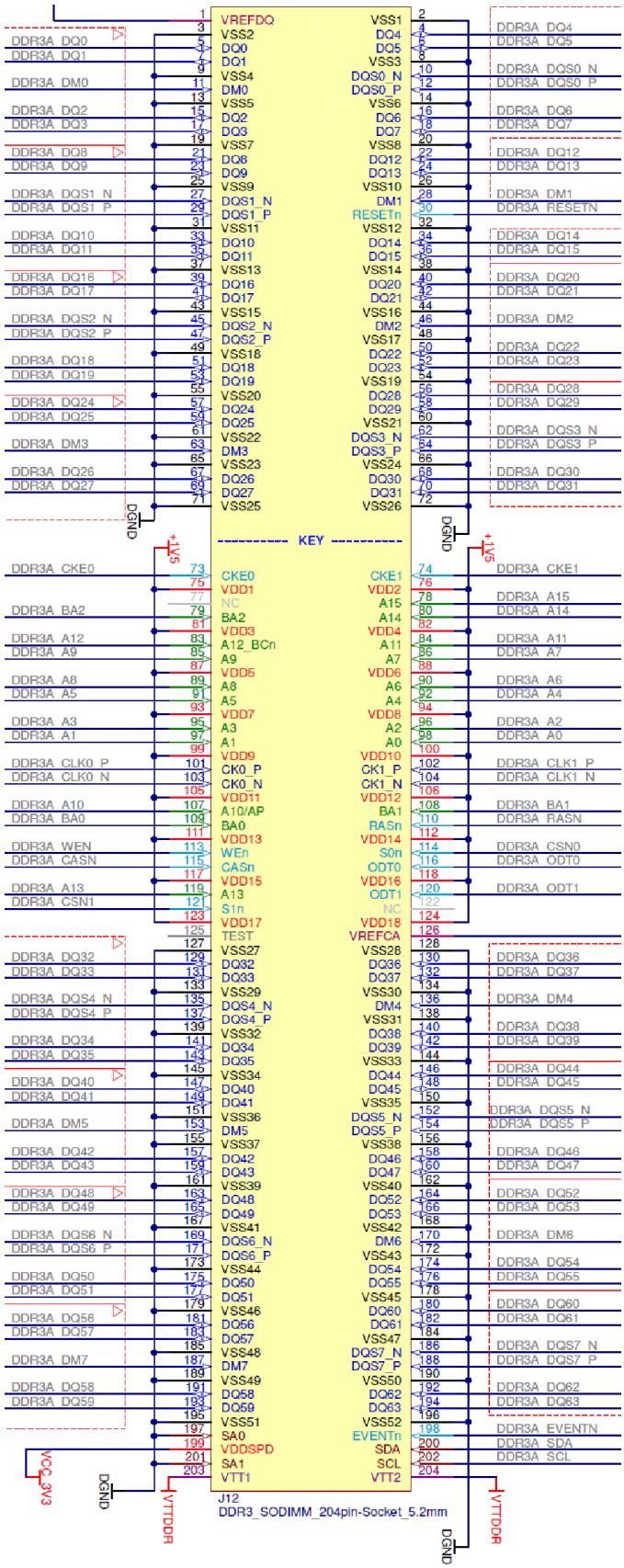

Table 30 J13 - DDR3 204pin SODIMM - DDR3 Interface B: Data[95..64]

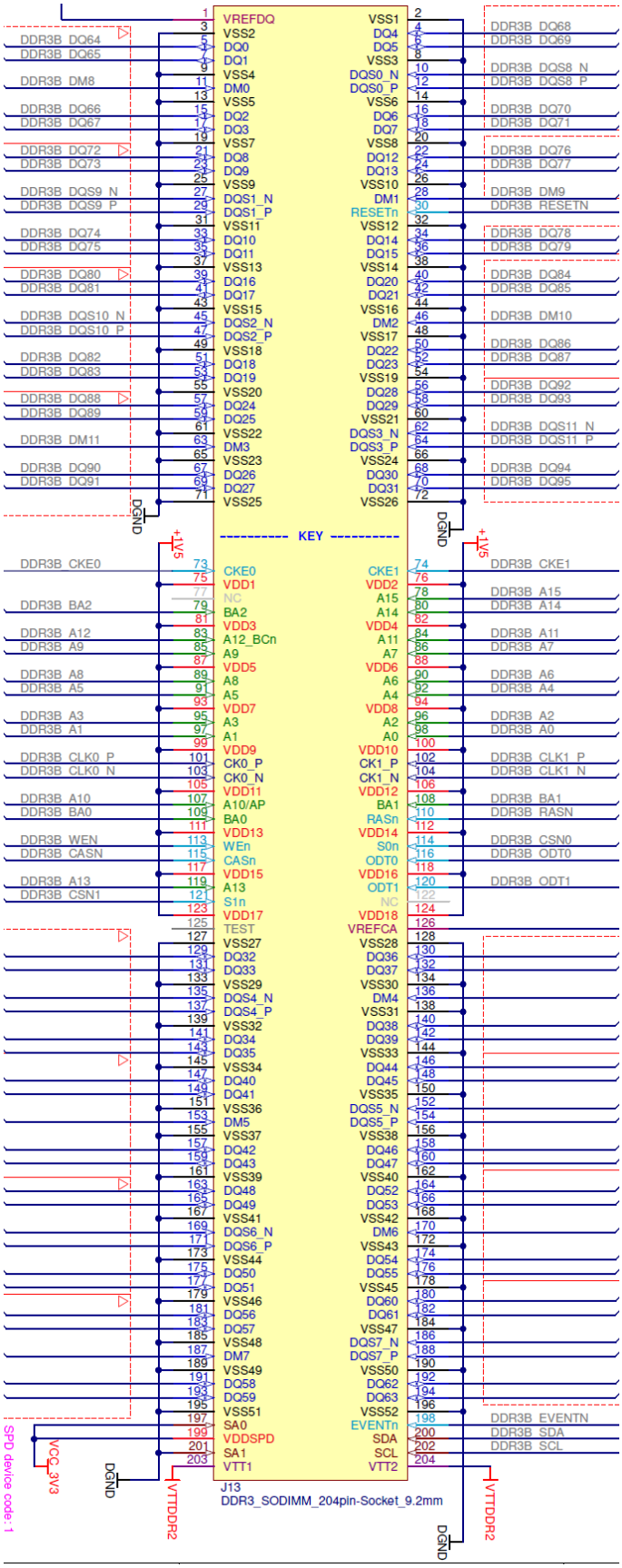

Table 31 J14 FPGA– JTAG Connector

FUNCTION	CONNECTOR PIN			FUNCTION
DGND	1	■	2	VCC_3V3
DGND	3	□	4	TMS
DGND	5	□	6	TCK
DGND	7	□	8	TDO
DGND	9	□	10	TDI
DGND	11	□	12	nc
DGND	13	□	14	nc

Table 32 J15 -PMBUS (Programming header for UCD9090 controller)

FUNCTION	CONNECTOR PIN			FUNCTION
nc	1	■	2	nc
nc	3	□	4	nc
nc	5	□	6	nc
PMBUS_CTRL	7	□	8	PMBUS_ALERT
PMBUS_CLK	9	□	10	PMBUS_DATA

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Table 33 J16 FMC Mezzanine Connector (extract from [RD1])

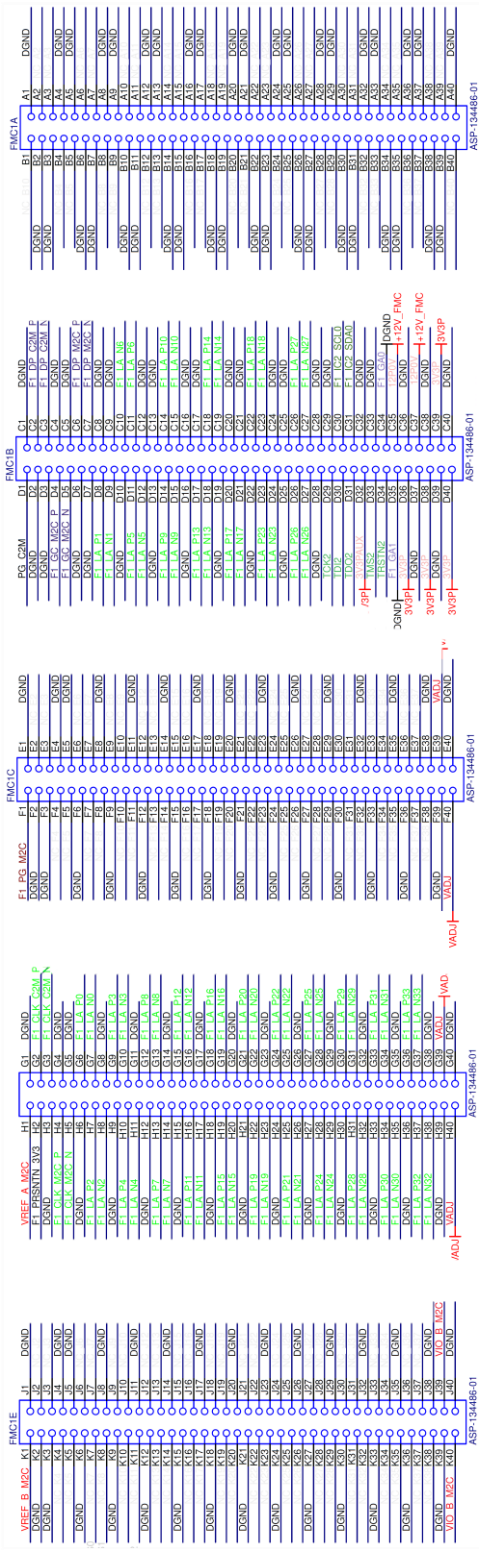

Table 34 J17 FAN – Connector

Pin	Name	Comment
1	**DGND**	Ground
2	+12V	Fan output +12V
3	-	No connect

Table 35 J18 POWER – External Power Connector for S/N 001,002,003

Pin	Name	Comment
1	**DGND**	Ground
2	+VIN	Power Input +12V, typically TBD A

Table 36 J19 SMAP-1 Header

FUNCTION	CONNECTOR PIN		FUNCTION
DGND	1	2	SMAP_INITN
DGND	3	4	SMAP_DONE
DGND	5	6	SMAP_PROGN
DGND	7	8	SMAP_RDWR
DGND	9	10	SMAP_CSIN
DGND	11	12	-
DGND	13	14	SMAP_SCLK
DGND	15	16	-

Table 37 J20 SMAP-2 Header

FUNCTION	CONNECTOR PIN		FUNCTION
DGND	1	2	SMAP_D0
DGND	3	4	SMAP_D1
DGND	5	6	SMAP_D2
DGND	7	8	SMAP_D3
DGND	9	10	SMAP_D4
DGND	11	12	SMAP_D5
DGND	13	14	SMAP_D6
DGND	15	16	SMAP_D7

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6.2 List of Headers

Table 38 *List of Headers & Jumpers*

Name	Function	Type	Description
JP1	GR716-GPIO0	3 pin header, 2mm	Pull-up = 1,2 Pull-down = 2-3
JP2	GR716-GPIO47	3 pin header, 2mm	Pull-up = 1,2 Pull-down = 2-3
JP3	GR716-GPIO62	3 pin header, 2mm	Pull-up = 1,2 Pull-down = 2-3
JP4	GR716-GPIO63	3 pin header, 2mm	Pull-up = 1,2 Pull-down = 2-3
JP5	GR716-DSUTX	3 pin header, 2mm	Pull-up = 1,2 Pull-down = 2-3
JP6	GR716-MOSI	3 pin header, 2mm	Pull-up = 1,2 Pull-down = 2-3
JP7	GR716-SCK	3 pin header, 2mm	Pull-up = 1,2 Pull-down = 2-3
JP8	GR716-SEL	3 pin header, 2mm	Pull-up = 1,2 Pull-down = 2-3
JP9	FPGA-MODE	2x3 pin header, 2mm	Install =Pull-up; Open = pull-down
JP10	SMAP	2x4 pin header, 2mm	1-2 = SMAP to GR716; 2-3 = SMAP to SPI PROM
JP11	I2CCP	2x4 pin header, 2mm	Backplane I2C pull-ups and connection to FPGA
JP12	SGPIO	2x4 pin header, 2mm	Backplane SGPIO pull-ups and connection toFPGA
JP13	FMC-JTAG2	2x4 pin header, 2mm	Connects FTDI Iinterface to FMC JTAG
JP14	GR716-DSU	2x4 pin header, 2mm	Connects FTDI Iinterface to GR716 DSU-UART
JP15	GR716-UART2	2x4 pin header, 2mm	Connects FTDI Iinterface to GR716 UART-2
JP16	SOCPIO0/RXD2	3 pin header, 2mm	Connects either SOCPIO0 or RXD2 to J9 pin 1
JP17	SOCPIO1/TXD2	3 pin header, 2mm	Connects either SOCPIO1 or TXD2 to J9 pin 2
JP18	WATCHDOG	2 pin header, 2mm	Connects GR716 Watchdog to Board Reset circuit

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6.3 List of Oscillators, Switches and LED's

Table 39 List of Oscillators and Crystals

Name	Function	Description
X1	GR716-CLK	20 MHz oscillator (soldered)
X2	GR716-SPWCLK	50 MHz oscillator (soldered)
X3	CLK2	DIL8socket for User Oscillator(freq:TBD)
X4	CLK3	300 MHz LVDS oscillator (soldered)
X5	MGT_CLK0	156.25 MHz LVDS oscillator (for GTH transceivers)
Y1	GR716-20MHz	GR716 XTAL (nof fitted)
Y2	FTDI-12MHz	12 MHz crystal (soldered) for FTDI interface
Y3	ETH0-25MHz	25 MHz crystal (soldered) for ETH0 PHY
Y4	ETH1-25MHz	25 MHz crystal (soldered) for ETH1 PHY

Table 40 List of Switches

Name	Function	Description
S1	RESET	Push Button Reset
S2	USR	Push Button – User Defined (connects to FPGA)
S3-1	GR-EN	DIP Switch :GR716 DSU enable (ON=’0’)
S3-2	GR-BREAK	DIP Switch : GR716 DSU BREAK (ON=’0’)
S3-3	SW0	DIP Switch : FPGA USR0 signal : User defined (ON=’0’)
S3-4	SW1	DIP Switch : FPGA USR0 signal : User defined (ON=’0’)
S3-5	SW2	DIP Switch : FPGA USR1 signal : User defined (ON=’0’)
S3-6	SW3	DIP Switch : FPGA USR2 signal : User defined (ON=’0’)
S3-7	SW4	DIP Switch : FPGA USR3 signal : User defined (ON=’0’)
S3-8	SW5	DIP Switch : FPGA USR5 signal : User defined (ON=’0’)
S4	ON-OFF	SP Slide
S5	PROG_B	Re-load FPGA Configuration

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Table 41 List of PCB mounted LED's

Name	Function	Description
D1a	POWER	3.3V power
D1b	USR0	FPGA USR0 signal
D2a	GR716-STATUS	GR716 GPIO57 signal
D2b	USR1	FPGA USR1 signal
D3a	SOC DONE	FPGA Done signal
D3b	USR2	FPGA USR2 signal
D4	+12V_BP	12V backplane voltage present
D5	VIN_ON	12V from backplane switched on to on-board circuits
D6	ETH_1V2_PG	ETH_1V2 regulator Power Good signal
D7	GTH_1V8_PG	GTH_1V8 regulator Power Good signal
D8	1V5PG	1V5 regulator Power Good signal
D9	VFMC_ON	FMC Voltage Status
D10	PM_3V3_PG	PM_3V3 regulator Power Good signal
D11	PG_C2M	Power Good Carrier to Mezzanine GPIO from UCD9090
D12	VCC_1V8_PG	VCC_1V8 regulator Power Good signal
D13	0V95PG	0V95 (Vcore) regulator Power Good signal
D14	GTH_1V0_PG	GTH_1V0 regulator Power Good signal
D15	VCC3V3PG	VCC3V3 regulator Power Good signal
D16	GTH_1V2_PG	GTH_1V2 regulator Power Good signal
D17	INIT_B	FPGA INIT state
D18	PROM_BUSY	Prom Busysignal

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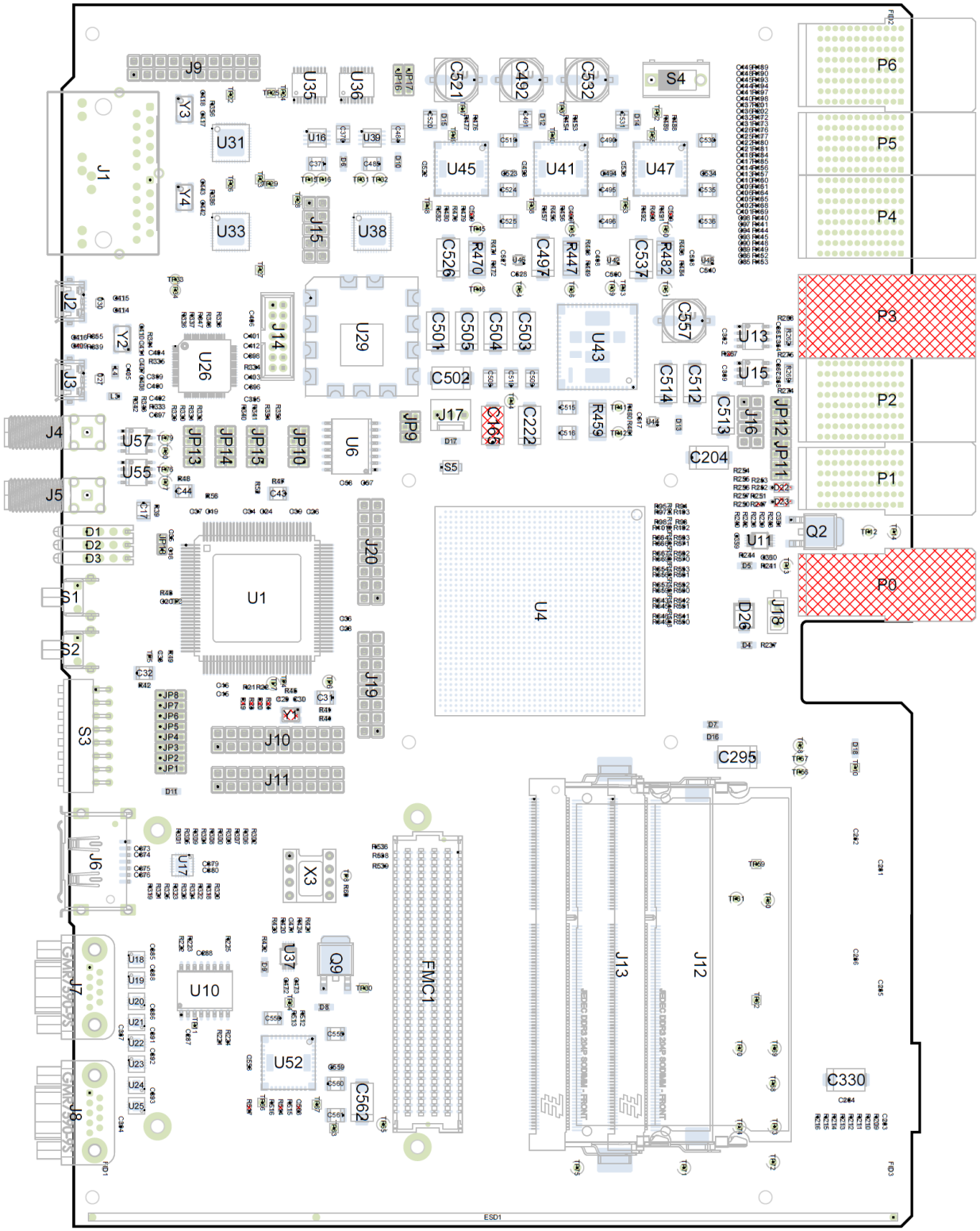

Figure 20 GR-CPCIS-XCKU PCB Top View (extract from [RD2])

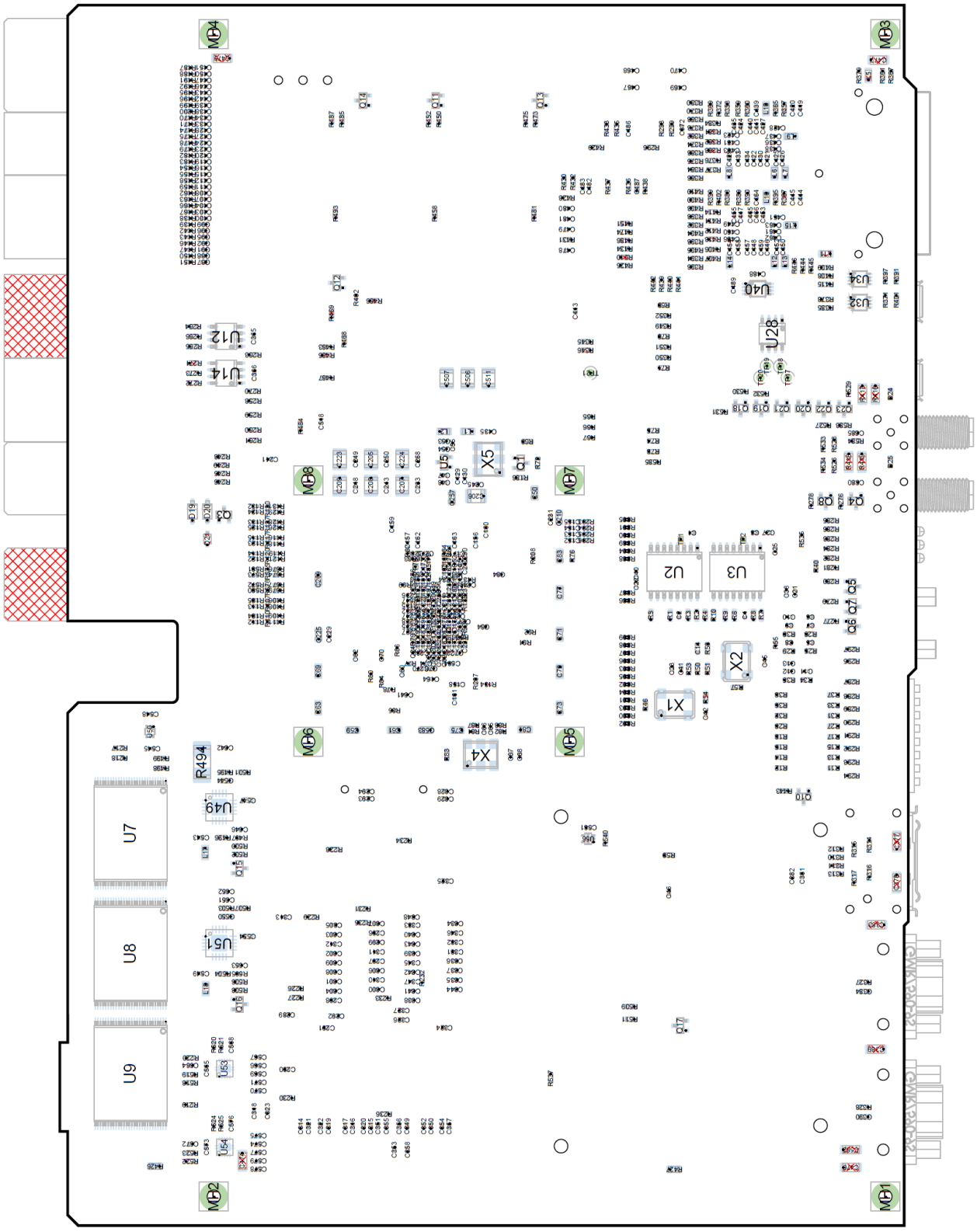

Figure 21 GR-CPCIS-XCKU PCB Bottom View (extract from [RD2])

REVISION INFORMATION

Issue	Date	Section / Page	Description
1.0	2022-01-26	All	New document
1.1	2022-02-08	All	Updated with review comments
1.2	2022-02-11	All	Converted to new CAES template. Added front page
1.3	2022-12-02	4.3	Clarified availability of board variants mounting larger FPGA devices. Clarified unused GTH banks.
1.4	2023-08-02	5.3	Modified default settings for JP9 and JP18
		All	Updated to Frontgrade branding
		3.2, 4.8	Clarified power-supply stand-alone usage. From S/N 004 of the board, the stand-alone power supply is provided through a Power Jack 2.1 mm SMD. Added warning about using the FPGA cooling fan before using the board.
1.5	2023-11-02	4.3	Clarified that board variants implementing the XCKU085-FLVA1517 FPGA are not manufactured.

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